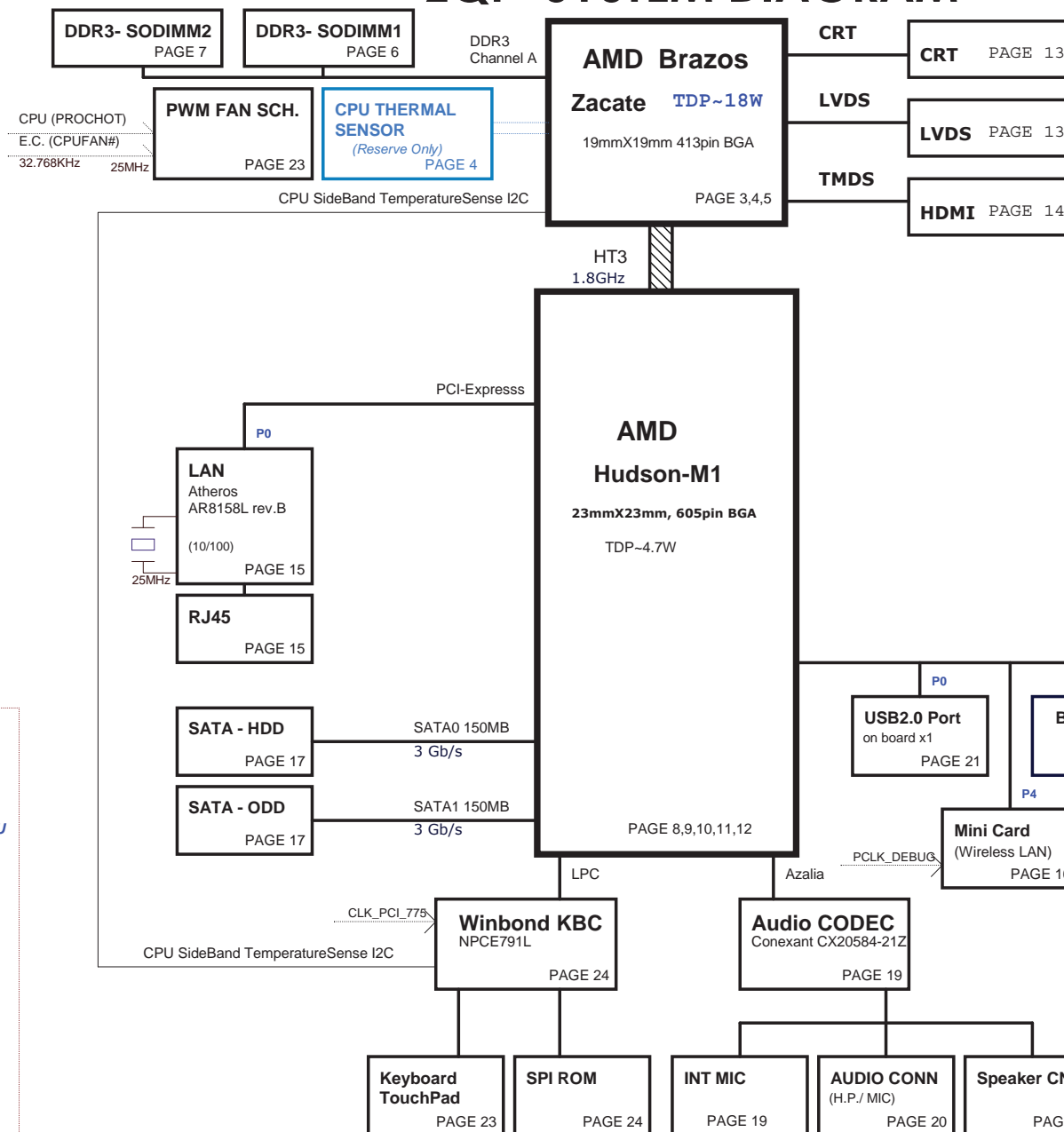


ZQP SYSTEM DIAGRAM

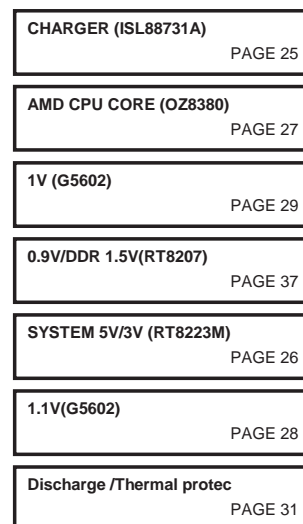


PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

HDMI@ ----> HDMI option
SP@ ----> Board ID/Strap pin
H@ ----> 家電下鄉

UMA REV: B

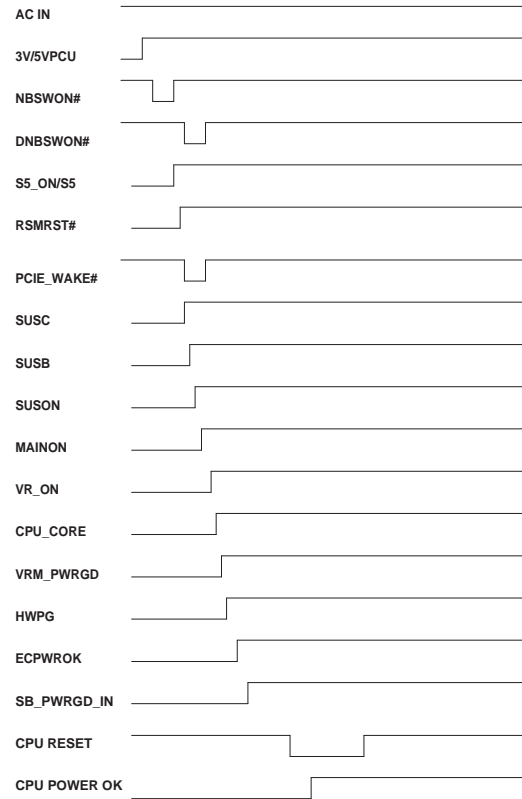


CPU

NB

PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/M(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD / ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT / TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

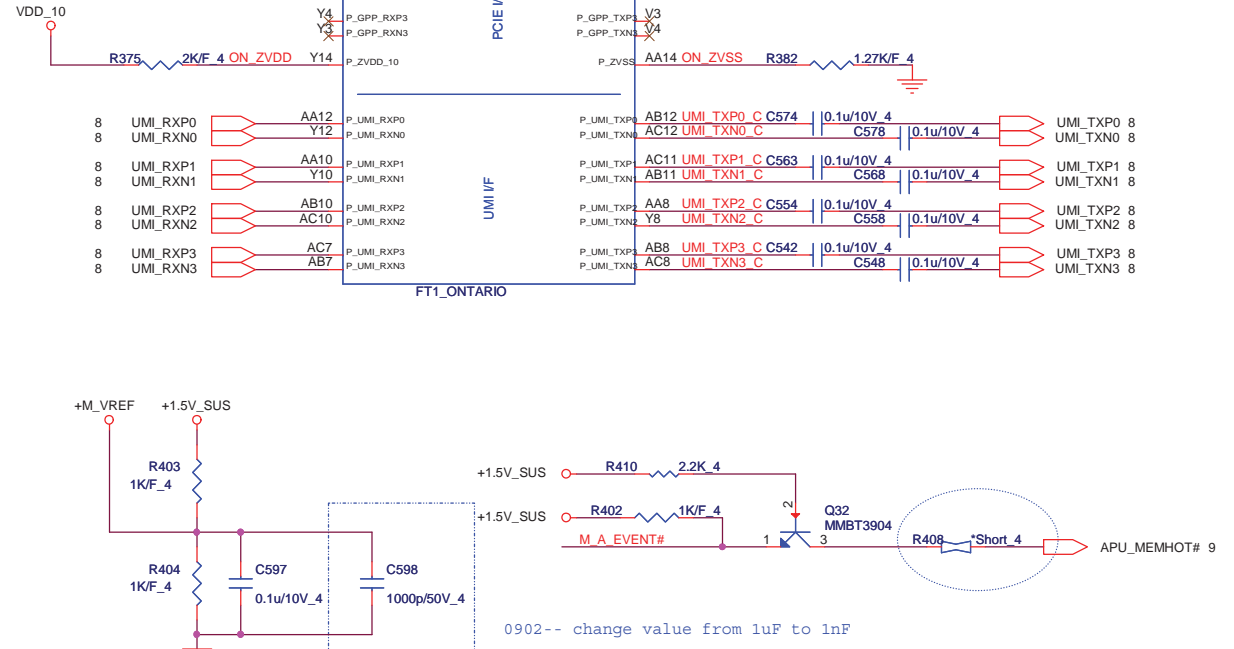
KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nila

Del PCIE TP 01/05

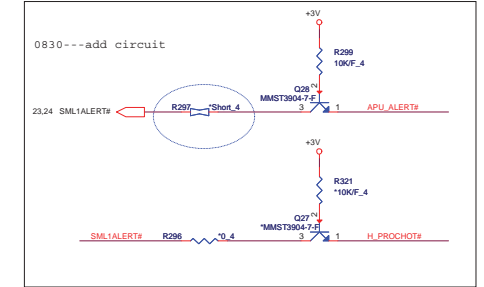
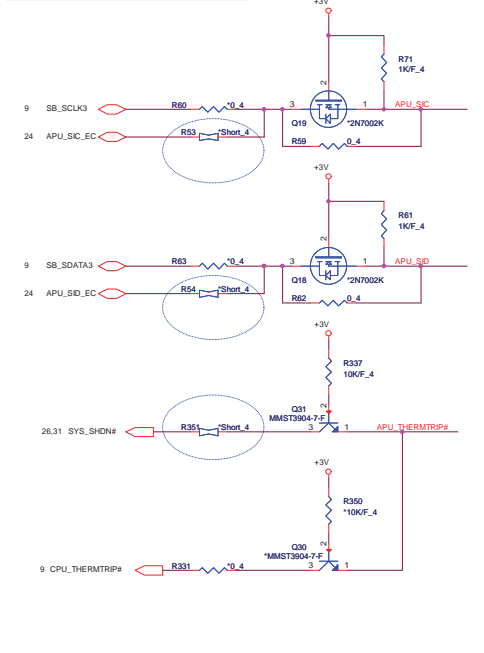
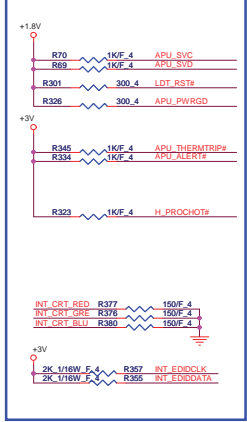
Del PCIE TP 01/05



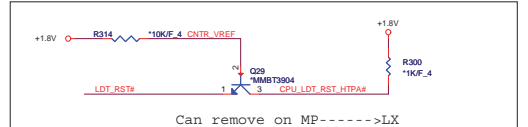
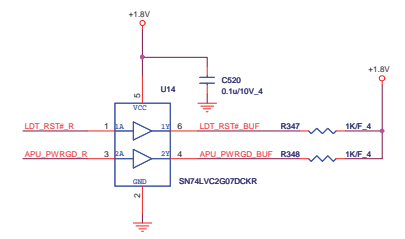
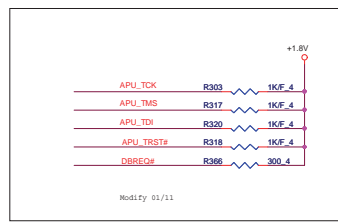
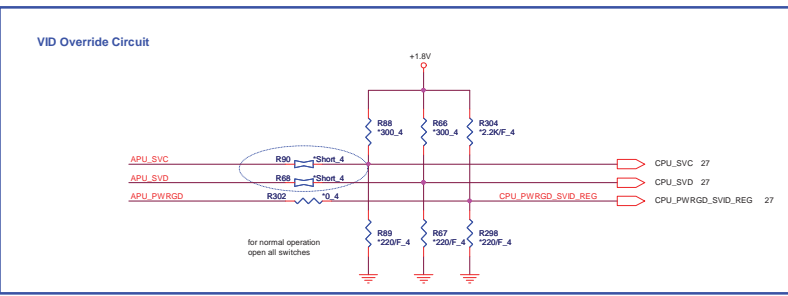
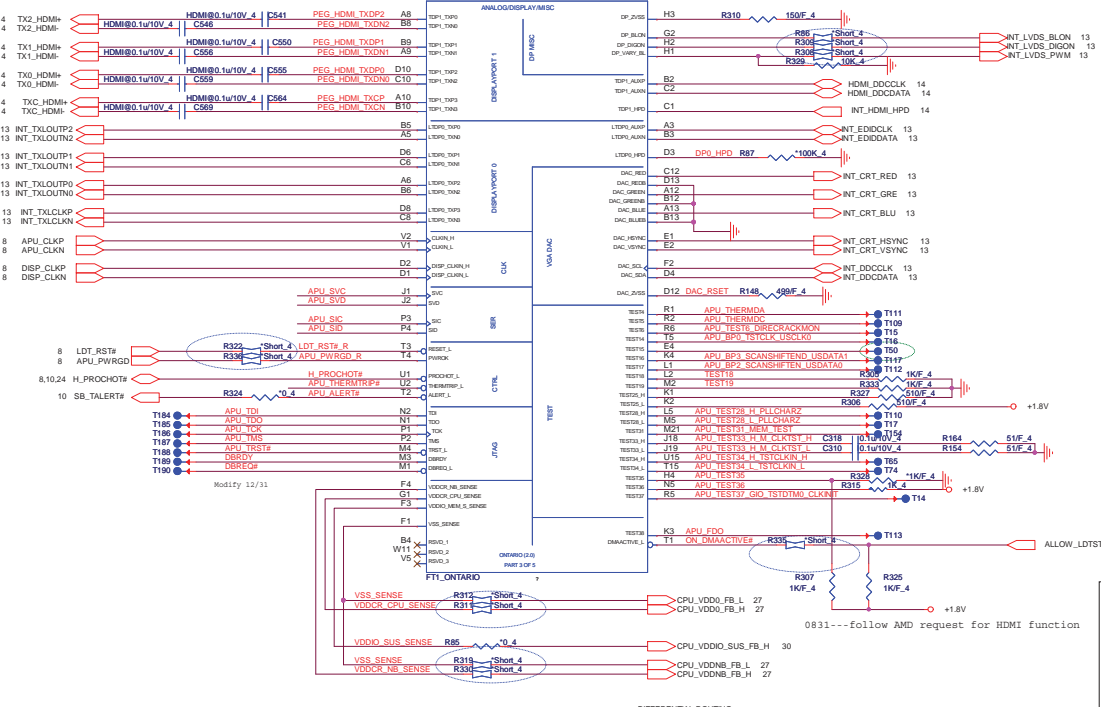
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	ONTARIO MEM & PCIE I/F(1/3)	1A
Date:	Tuesday, March 15, 2011	Sheet 3 of 32

E350	AJ0E350VT01
C50	AJ00C50VT02



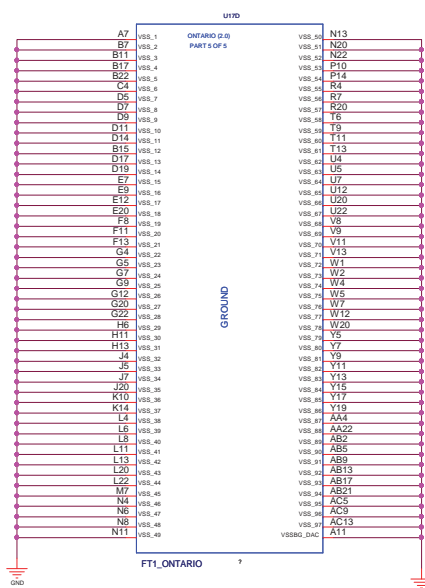
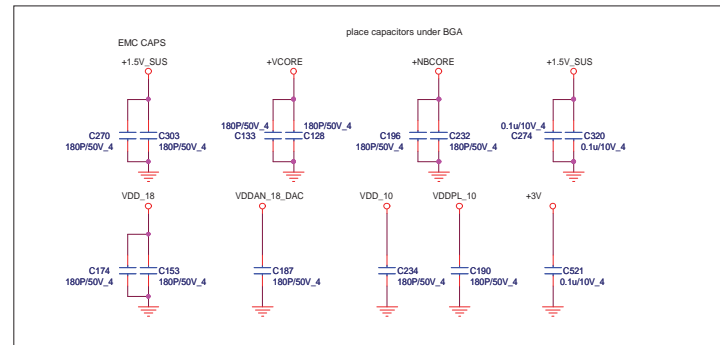
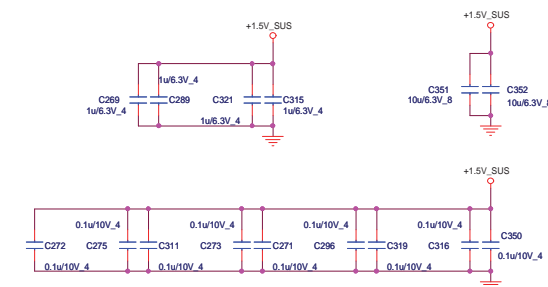
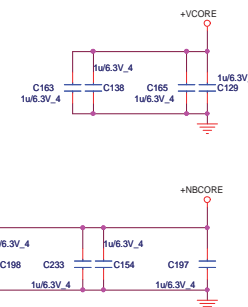
ASB HDMI 01/18








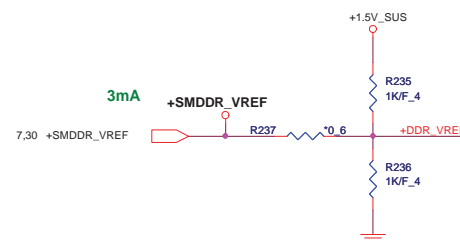
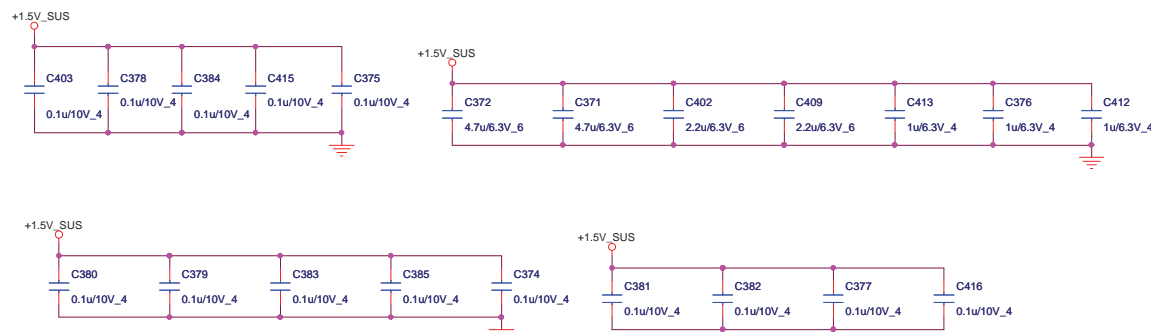
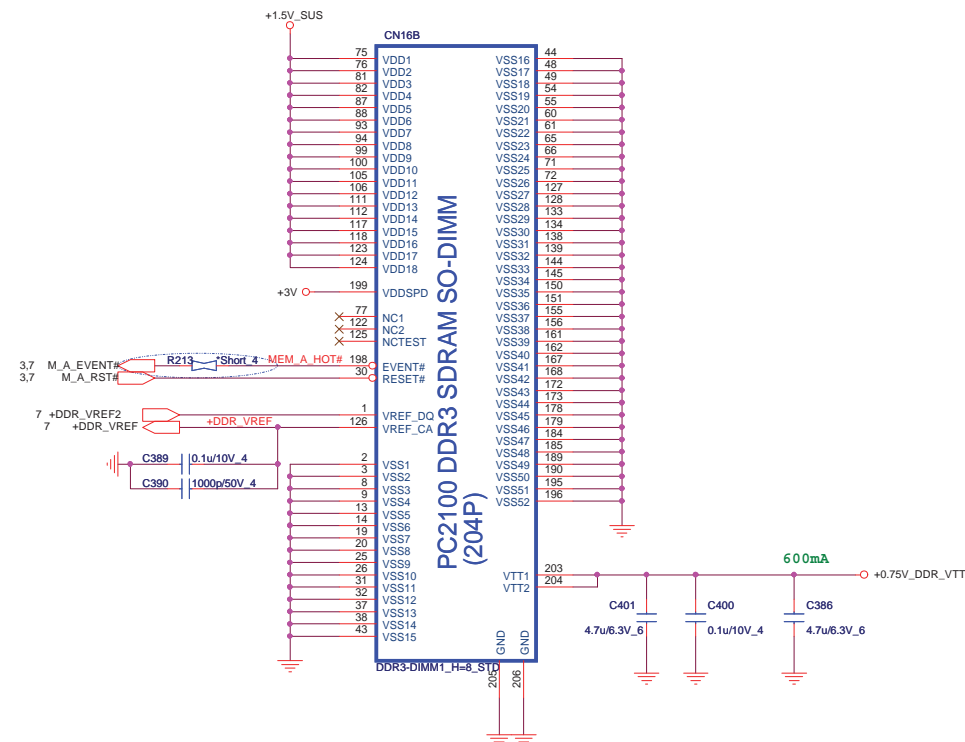
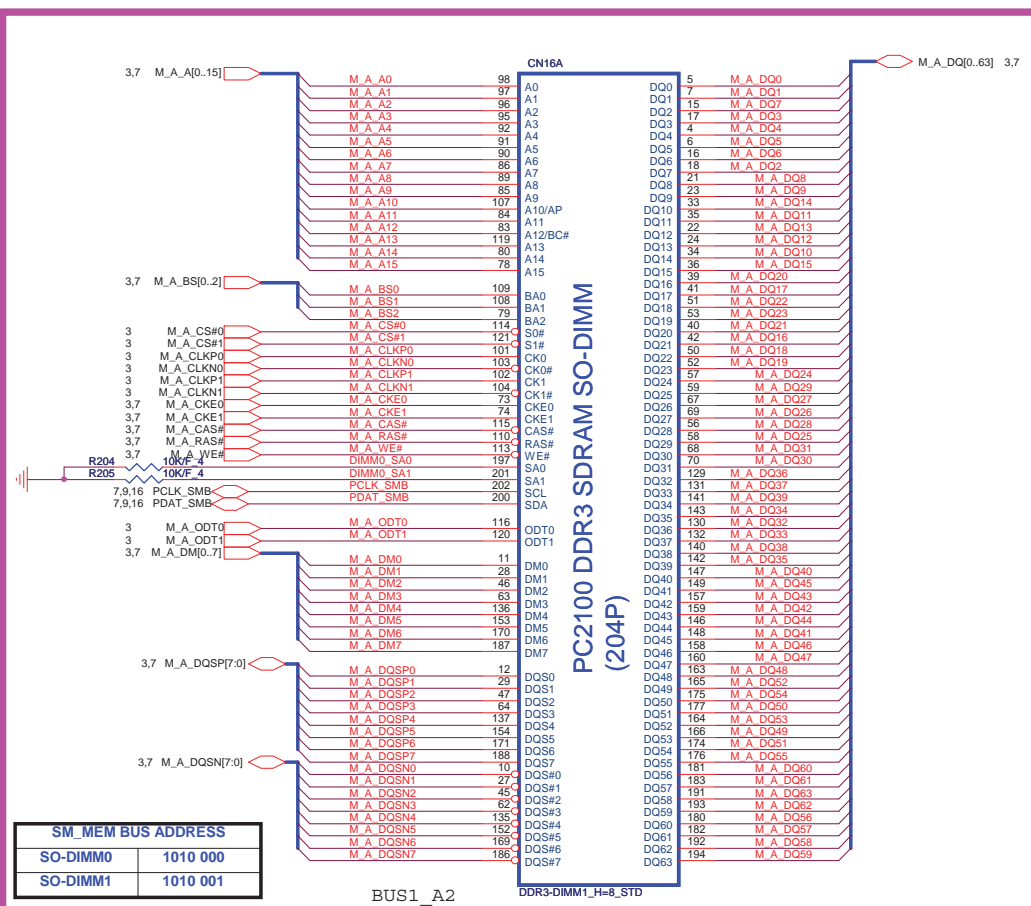
PROJECT : QZP
Quanta Computer Inc.

Size	Document Number	Rev
	ONTATIO DISPLAY/CLK/MI(2/3)	1A
Date:	Tuesday, March 15, 2011	Sheet 4 of 32



0830--P/N and footprint are follow ZR7B

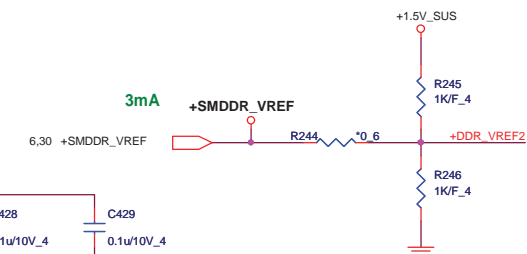
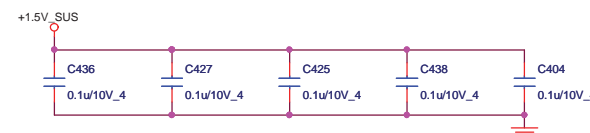
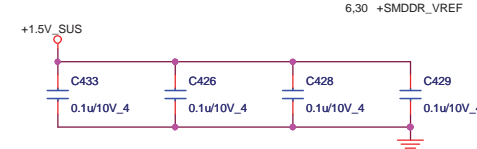
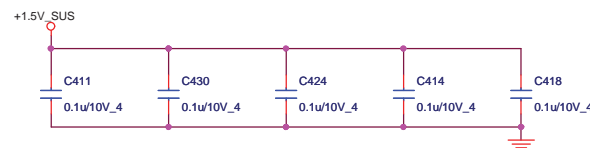
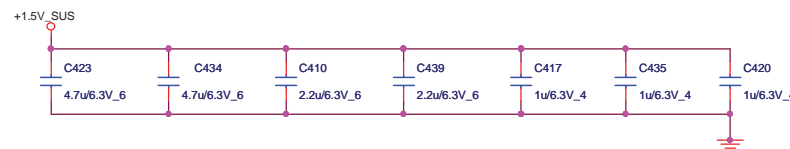
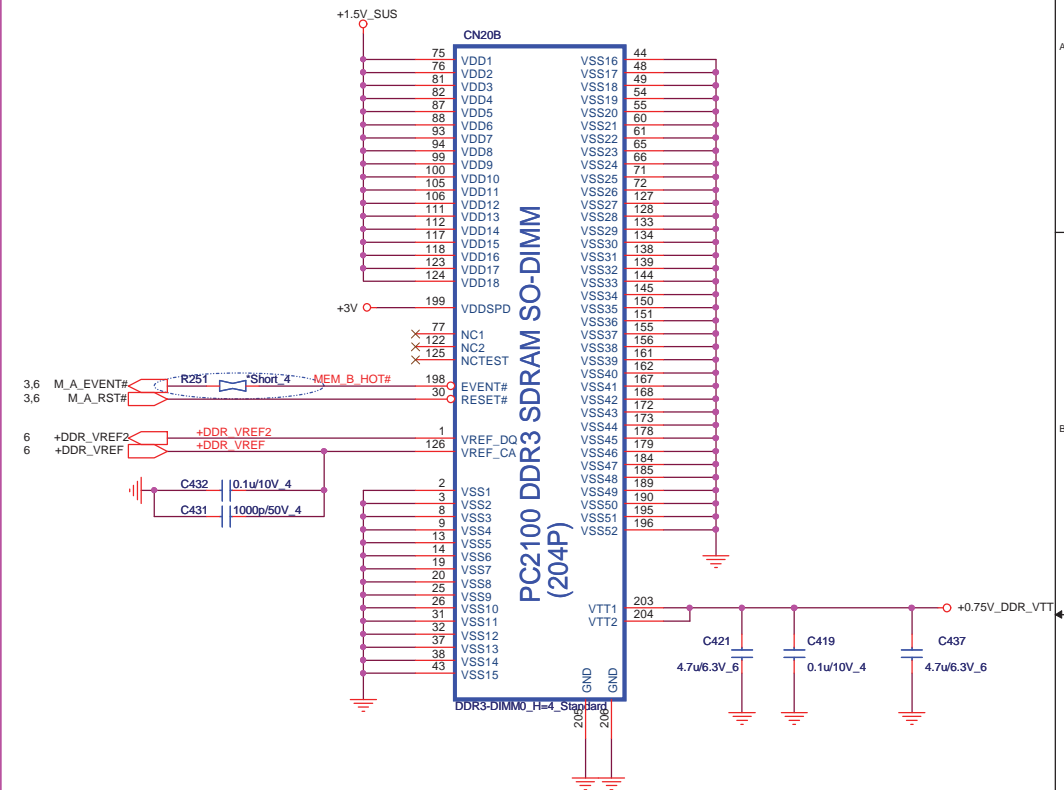
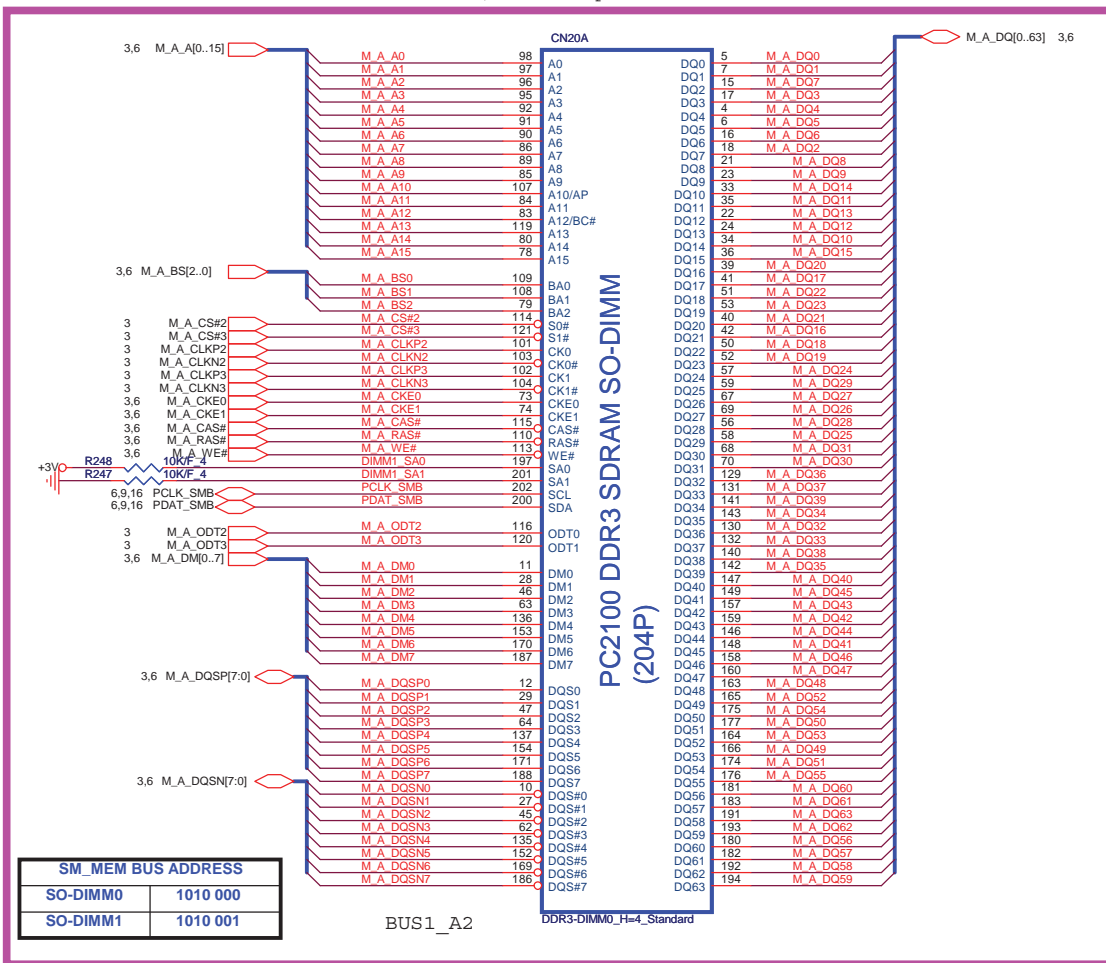
 +1.5V_SUS 3,5,7,22,30
 +0.75V_DDR_VTT 7,30
 +3V 4,5,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31



PROJECT : ZQP
Quanta Computer Inc.

Size Document Number
DDR3 SO-DIMM (STD) Rev 1A

Date: Tuesday, March 15, 2011 Sheet 6 of 32



PLACE SATA AC COUPLING
CAPS CLOSE TO Hudson M1

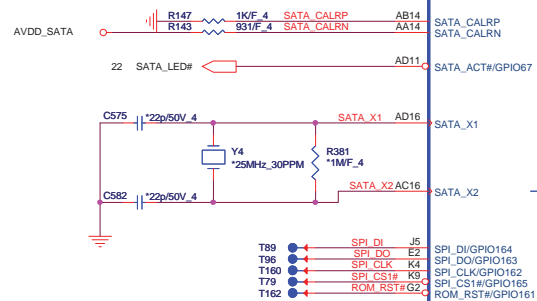
SATA ODD



PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF Hudson M1

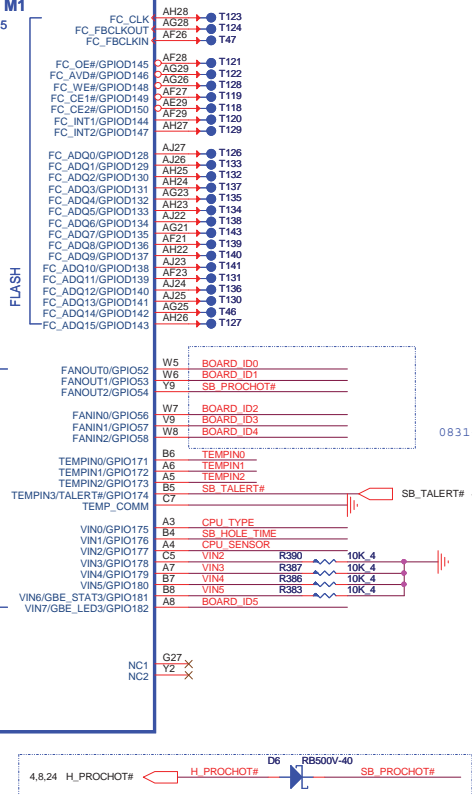
```
XTLVDD_SATA-- SATA
crystal power

PLVDD_SATA--
SATA_PLL
POWER
```



Hudson M1

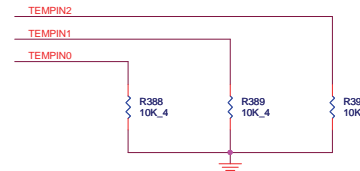
Part 2 of 5



0831--add circuit

This page is different AMD Nile

AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.

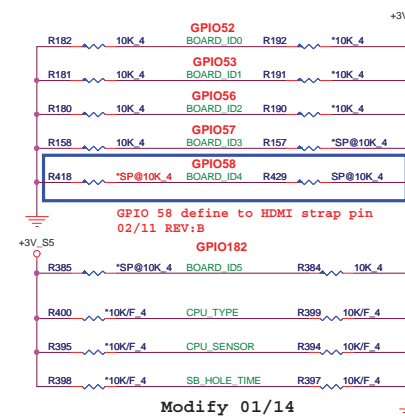


0831--modify location

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0
SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0
DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO57
(Dis) SW	1
UMA	0
	GPIO58
With HDMI	1
Without HDMI	0
	GPIO18:
PX4.0	1
PX3.0	0



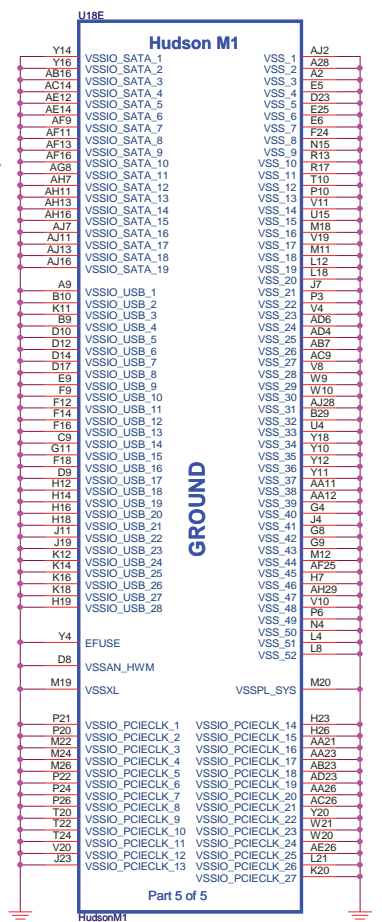
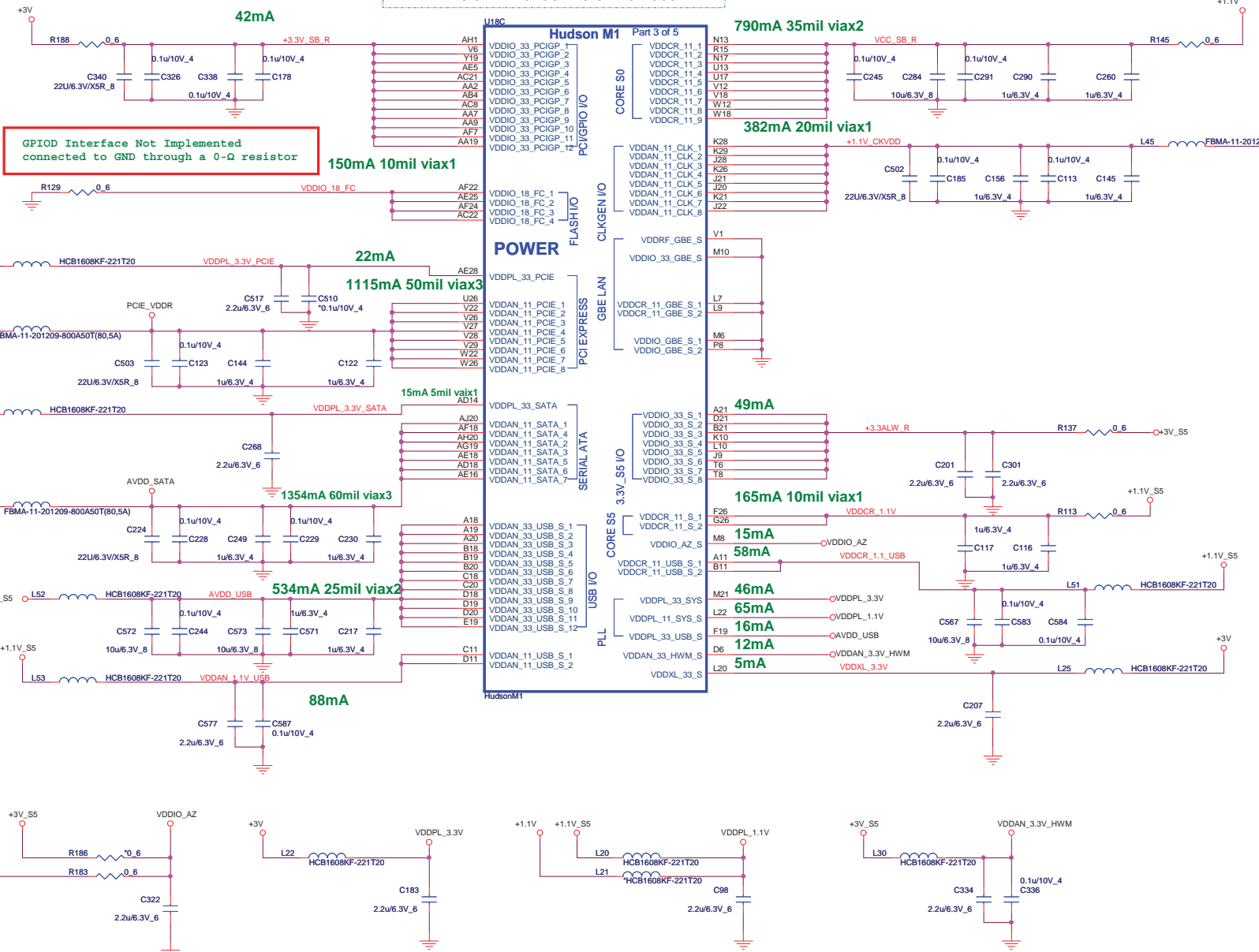
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON SATA/BIDS(3/5)	1A
Date:	Tuesday, March 15, 2011	Sheet 10 of 32

This page is different AMD Nile

+3V 4,5,6,7,9,10,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31
 +1.1V 22,28,31
 +3V_S5 8,9,10,12,15,21,22,26
 +1.1V_S5 28
 AVDD_SATA 10
 VDDIO_AZ 12

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

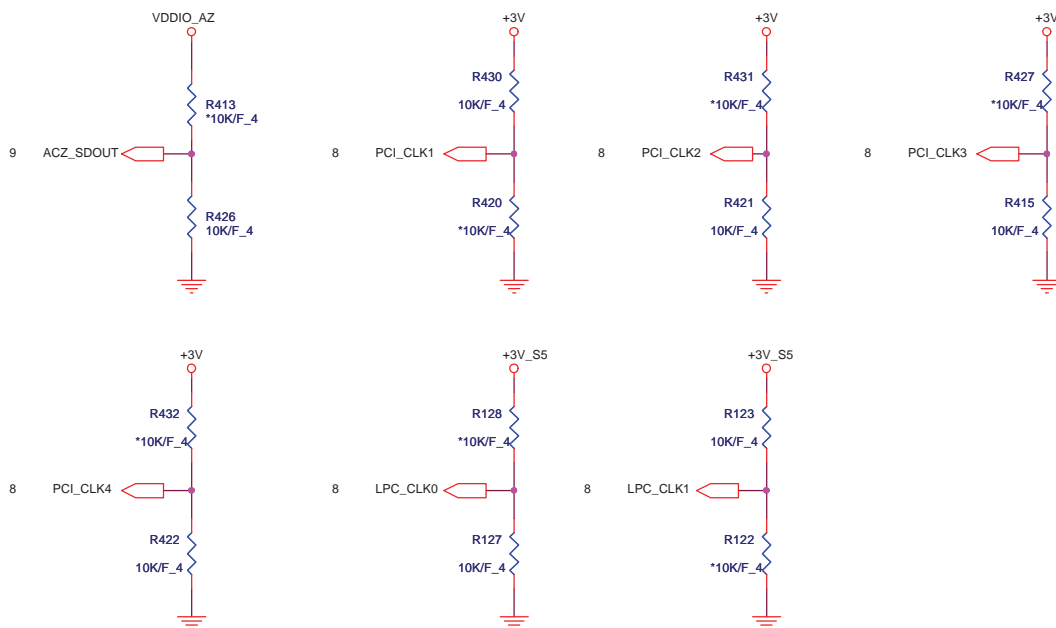




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

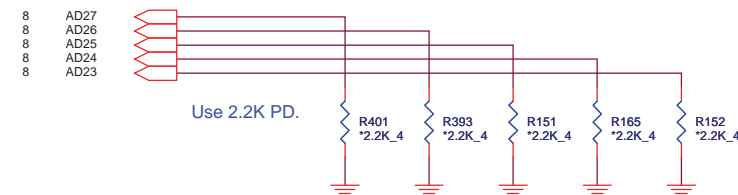


VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



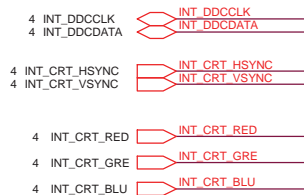
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



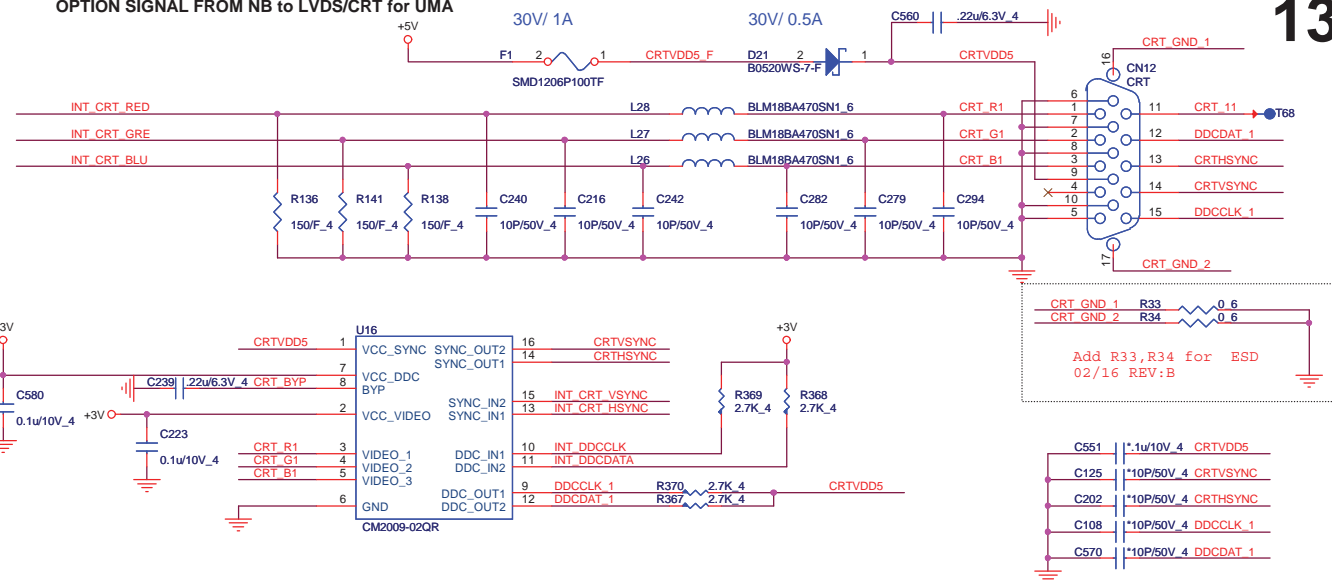
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date:	Tuesday, March 15, 2011	Sheet 12 of 32

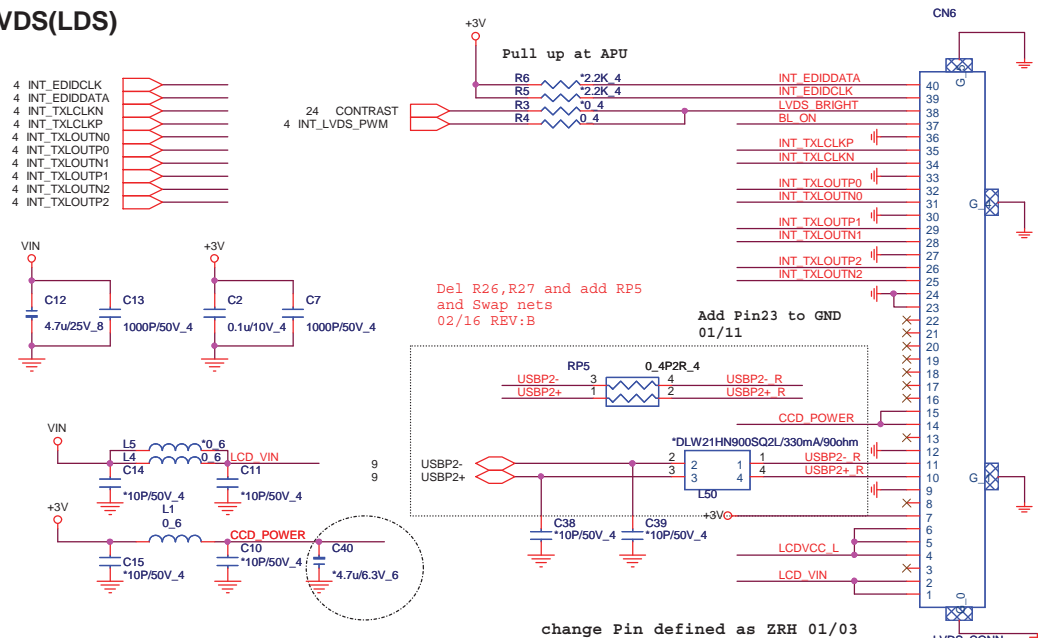
CRT



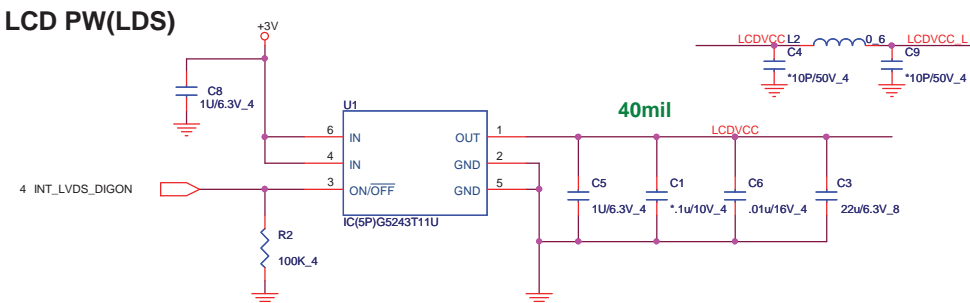
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



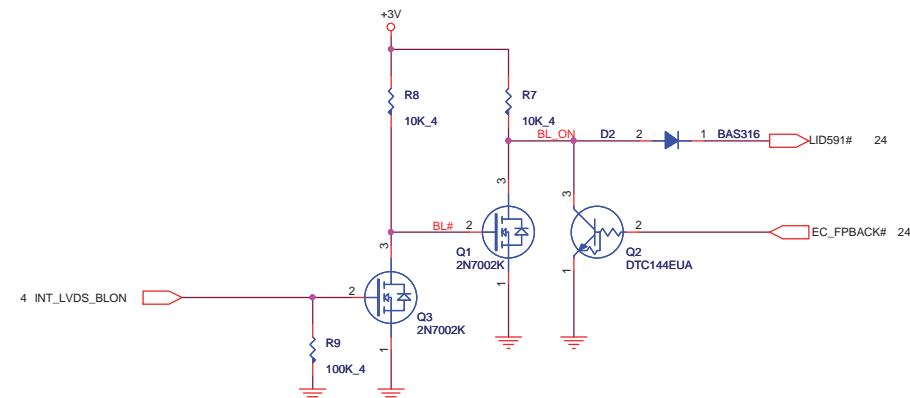
LVDS(LDS)



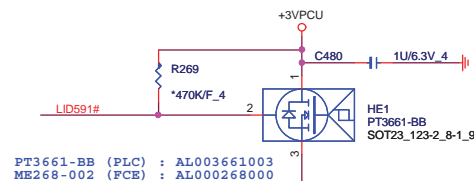
LCD PW(LDS)



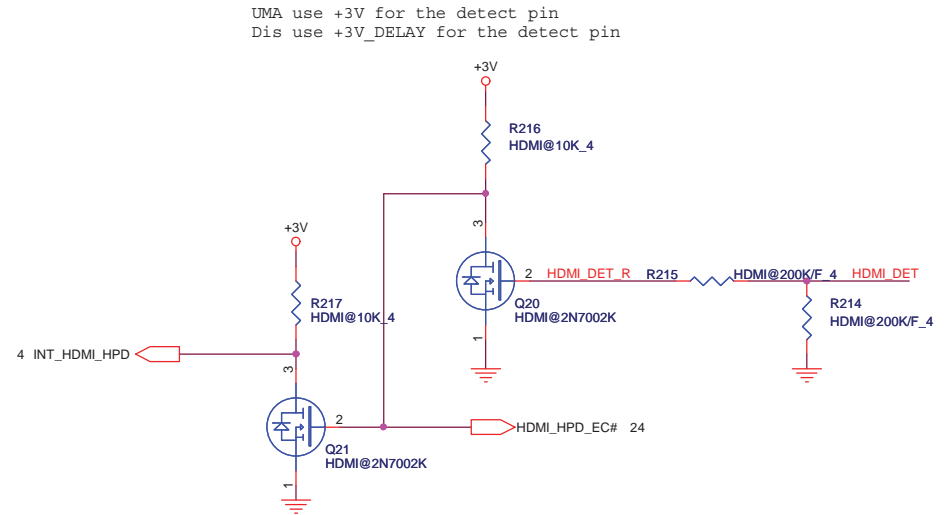
Backlight Control(LDS)



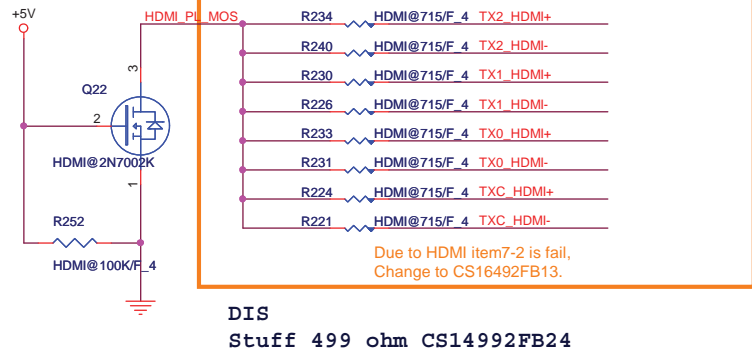
Lid Switch (HSR)



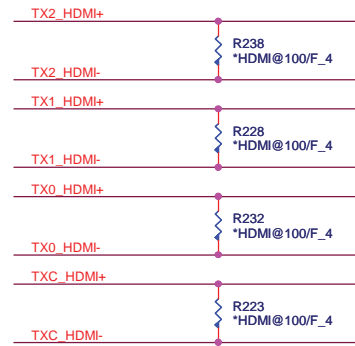
4 HDMI_DDCDATA HDMI_DDCDATA
4 HDMI_DDCCLK HDMI_DDCCLK



Close to HDMI Connector

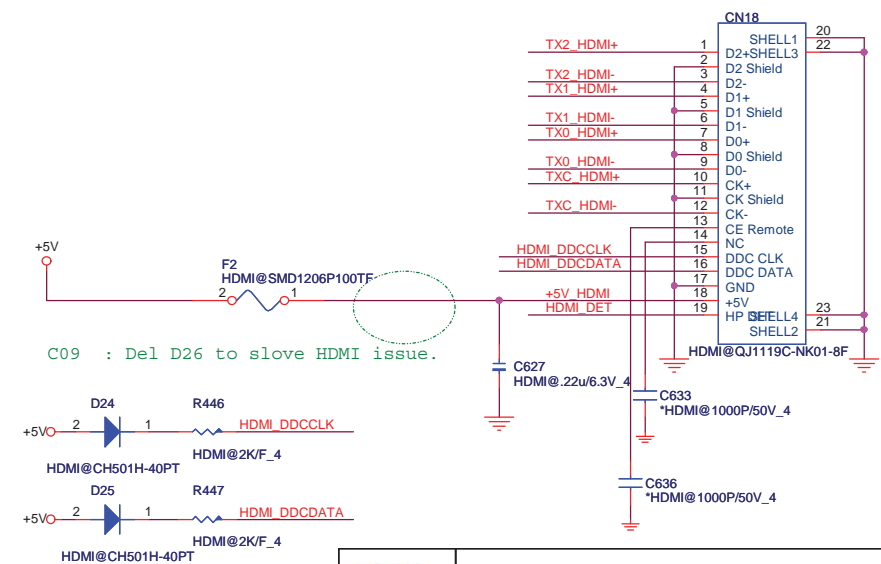


Close connector



Added HDMI function
01/19 REV:B

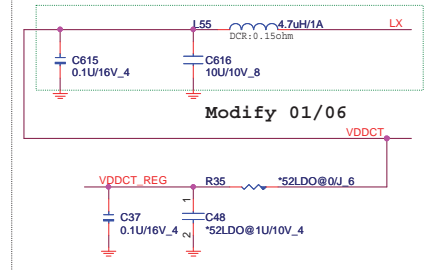
HDMI PORT (HDM)



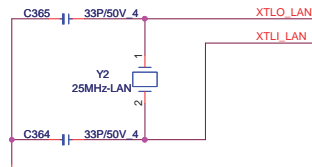
<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@

<Layout note>
Close to Pin1

If use LDO mode L55 no stuff

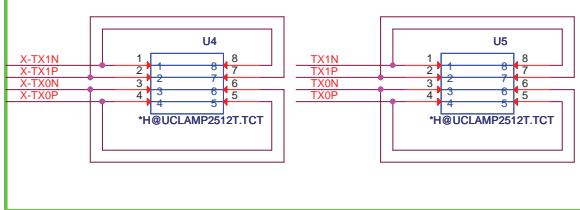


Modify 01/06



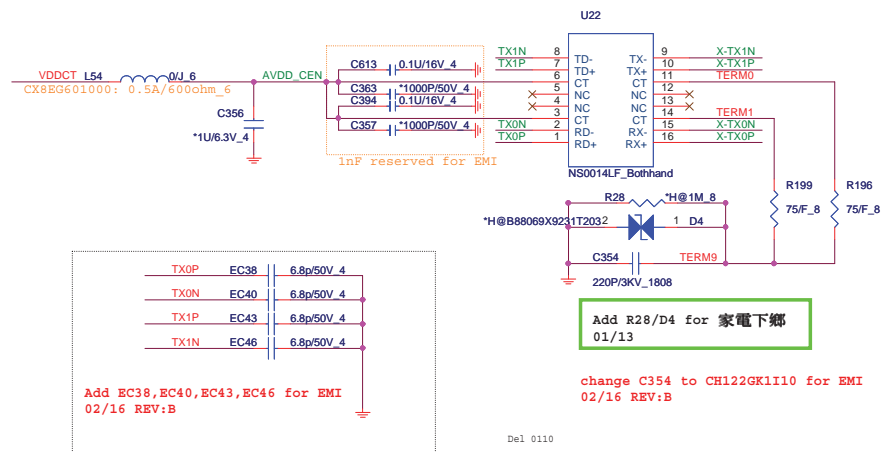
BG625000486

Add R28/D4 for 家電下鄉
01/13



TRANSFORMER (LAN)

exchange pair 0/1
0110



Del 0110

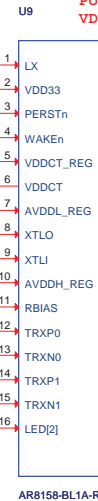
Add R28/D4 for 家電下鄉
01/13

change C354 to CH122GK110 for EMI
02/16 REV:B

* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

Power Sequence:
VDD33 to PERSTn >= 100ms

AR8158
4X4mm
32Pin QFN



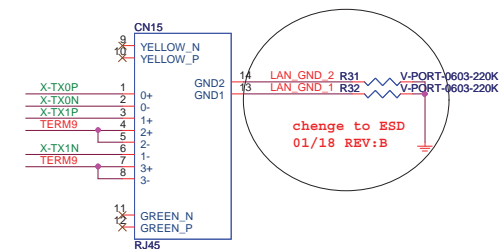
+3V_S5 — 2 — VDD33
+1.1V analog power — 24/27 — AVDDL
+1.7V analog power — 6 — VDDCT

ATHEROS
AR8158

AVDDL_REG — 7 — +1.1V regulator output (For all the analog 1.1V supply pins)
AVDDH_REG — 10 — +2.7V regulator output
DVDDL_REG — 30 — +1.1V regulator output (For all the digital 1.1V supply pins)
VDDCT_REG — 5 — +1.8V regulator output (For VDDCT when LDO mode)
LX — 1 — +1.7V Switching regulator (For VDDCT when switching mode)

RJ45 Connector (LAN)

Del LAN LED 01/05



change RJ45 connector without LED
03/02

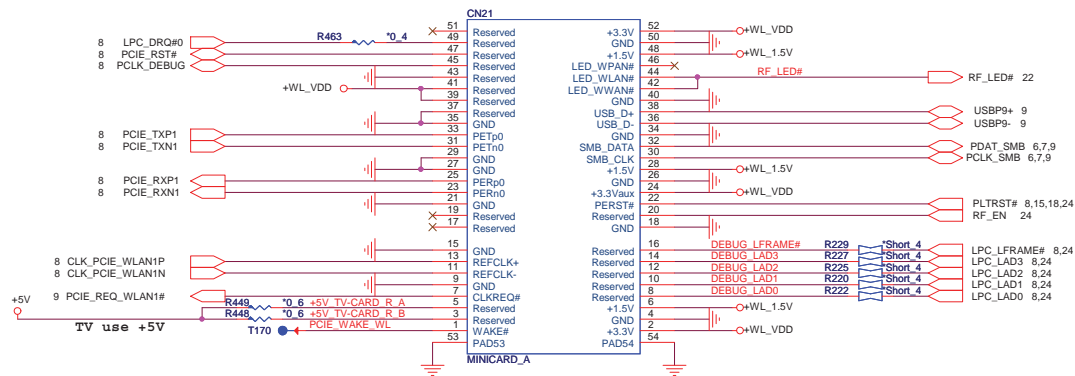
We will change RJ45 connector

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev
	LAN AR8158L	1A
Date:	Tuesday, March 15, 2011	Sheet 15 of 32

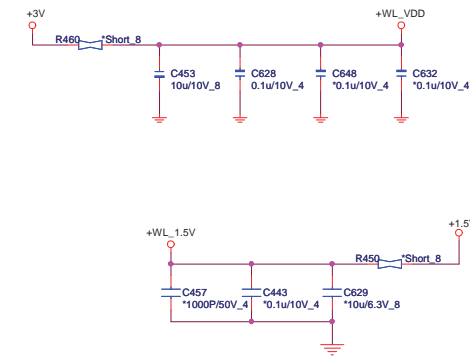
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



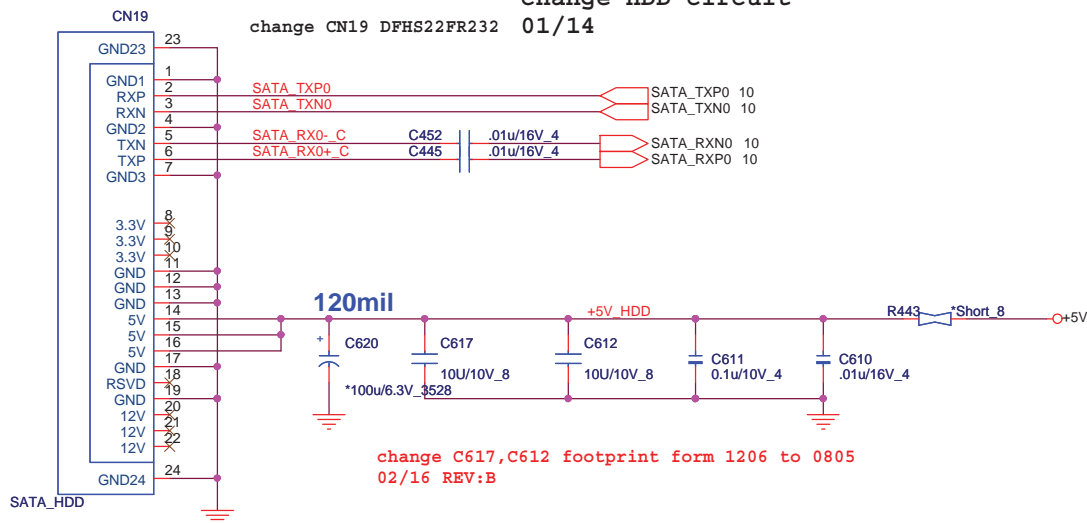
Debug



SATA HDD

change HDD circuit

change CN19 DFHS22FR232 01/14

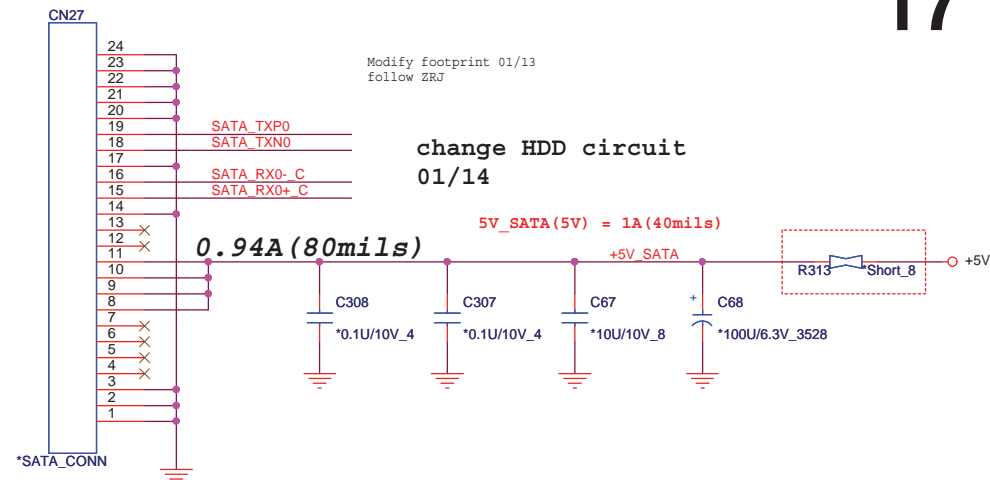


SATA HDD(HDD)

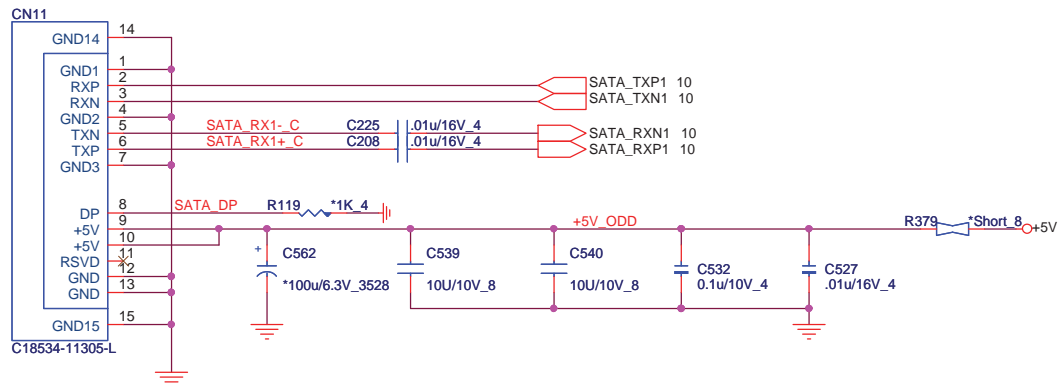
17

Modify footprint 01/13
follow ZRJ


change HDD circuit
01/14



SATA ODD



change C539,C540 footprint form 1206 to 0805
02/16 REV:B

			PROJECT : ZQP Quanta Computer Inc.	
Size	Document Number		Rev	
	SATA-HDD/ODD/HOLE		1A	
Date:	Tuesday, March 15, 2011	Sheet	17 of	32

CARD READER Controller AU6435-GDL

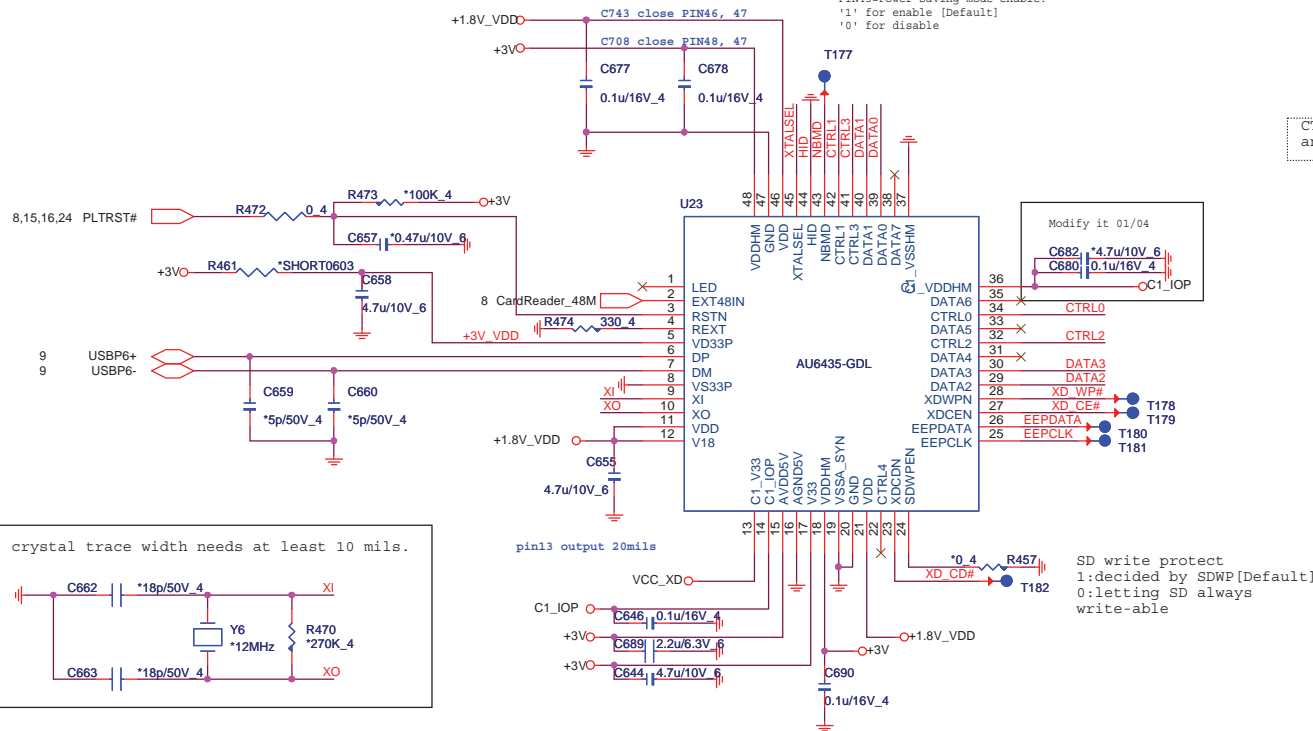
2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033

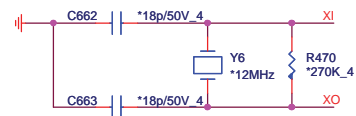
PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

R464 0.4 XTALSEL

PIN43=Power saving mode enable.
'1' for enable [Default]
'0' for disable

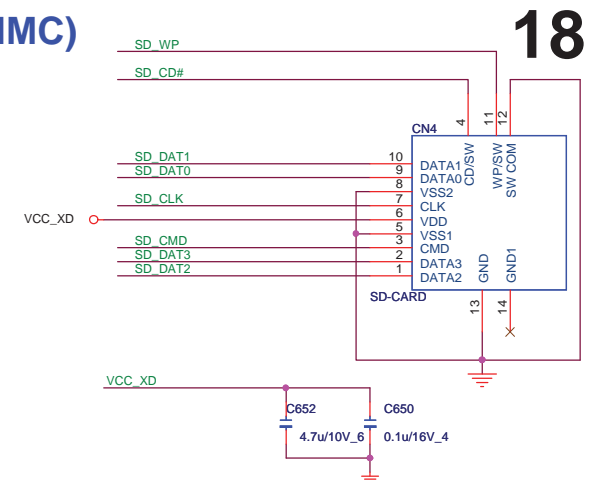


crystal trace width needs at least 10 mils.



pin13 output 20mils

SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able



Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

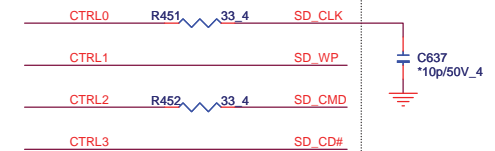
CTRL0, CTRL1 trace length shorter ,
and surround with GND.

The trace length difference for each card interfaces should be
smaller than 500 mil



Close to connector

CLK length should be as short as possible. Shorter than
1200 mil is good.



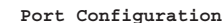
change R452 from CTRL1 to CTRL2
01/13

<http://hobi-elektronika.net>

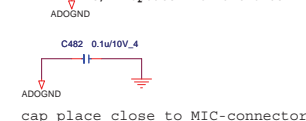



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AU6435 CardReader	1A
Date:	Tuesday, March 15, 2011	Sheet 18 of 32

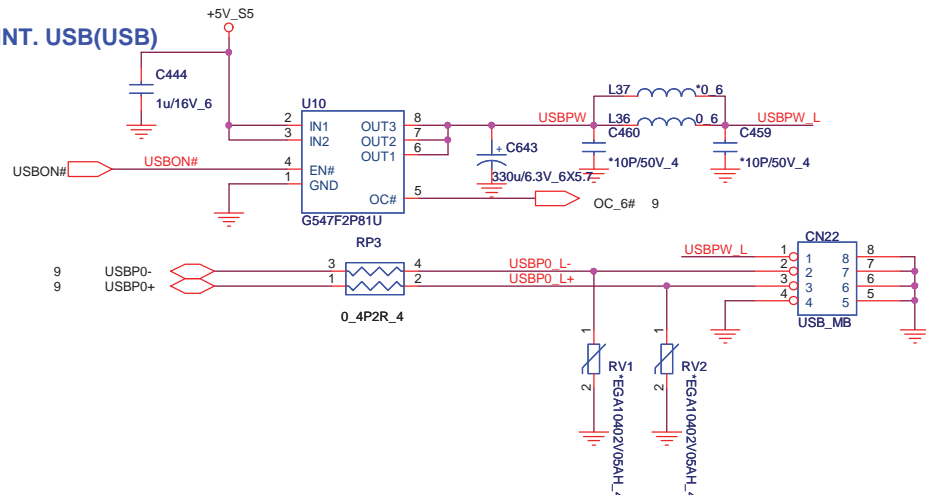


Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/Li/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

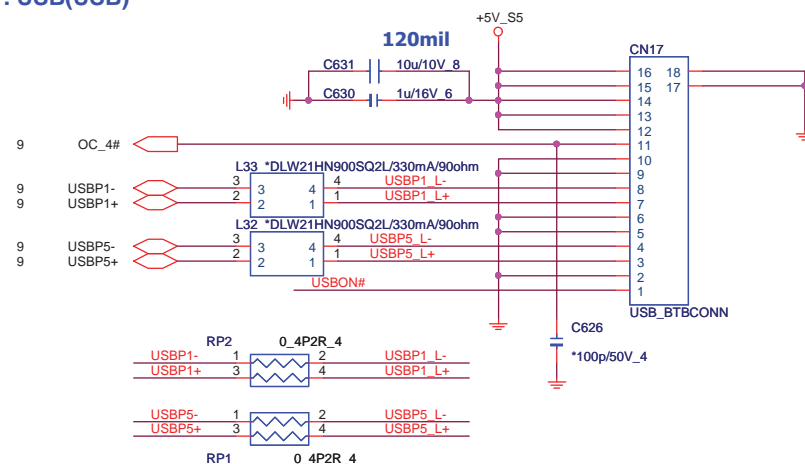


	PROJECT : ZQP Quanta Computer Inc.		
	Size	Document Number	Rev
	CONEXANT 20584		1A
Date:	Grandeur March 16 2011	Echant	10 of 22

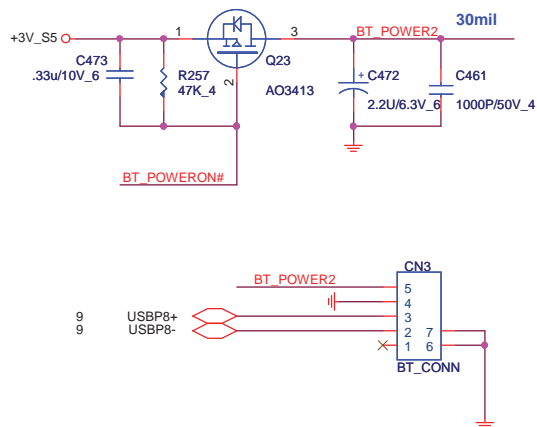
INT. USB(USB)



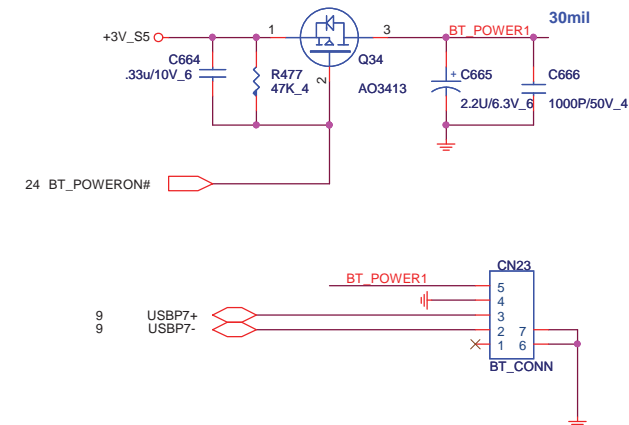
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



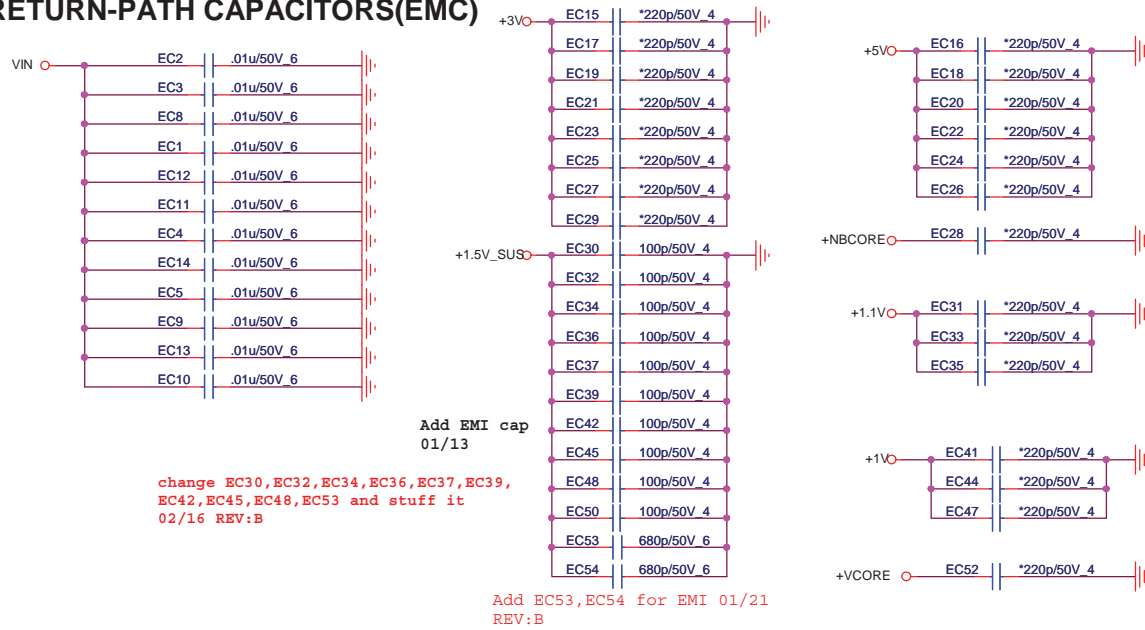
BLUETOOTH V3.0 CONN(BTM)



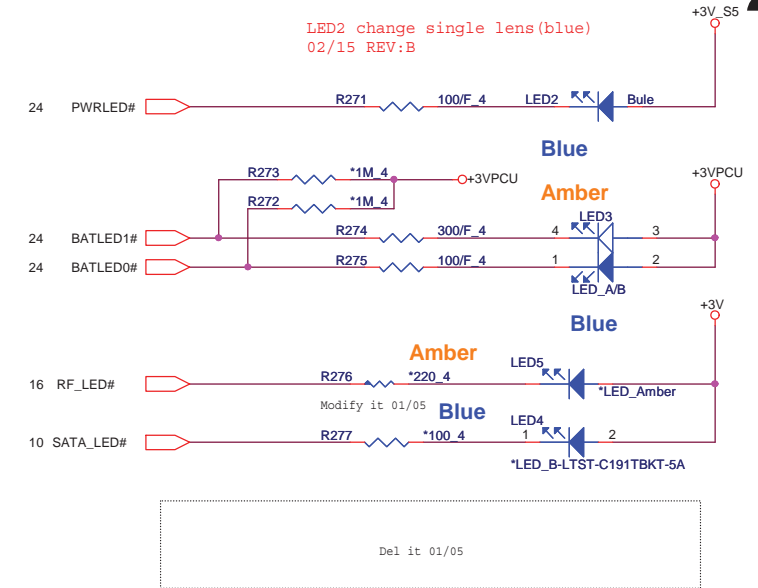
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT	1A
Date:	Tuesday, March 15, 2011	Sheet 21 of 32

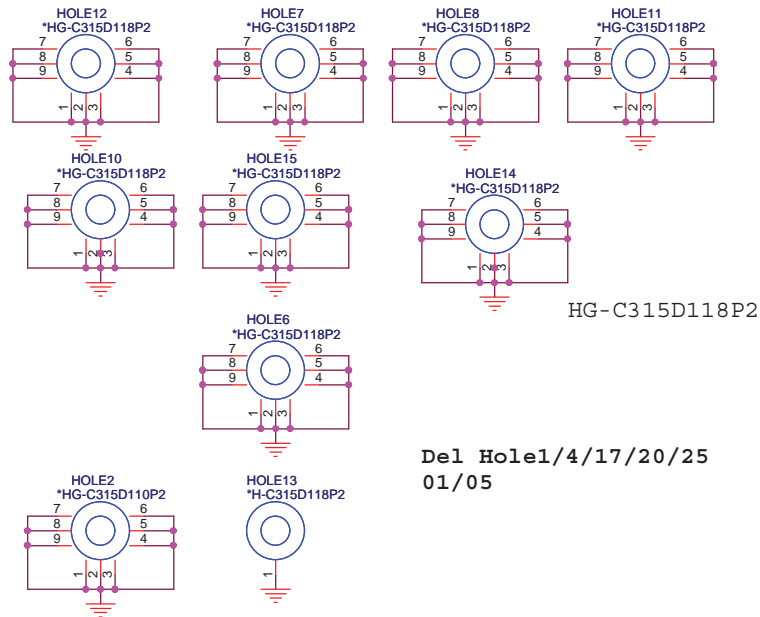
EE RETURN-PATH CAPACITORS(EMC)



LED(UIF)



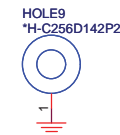
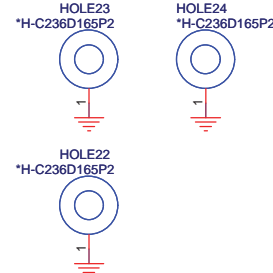
HOLE(OTH)



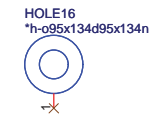
mini PCI



cpu



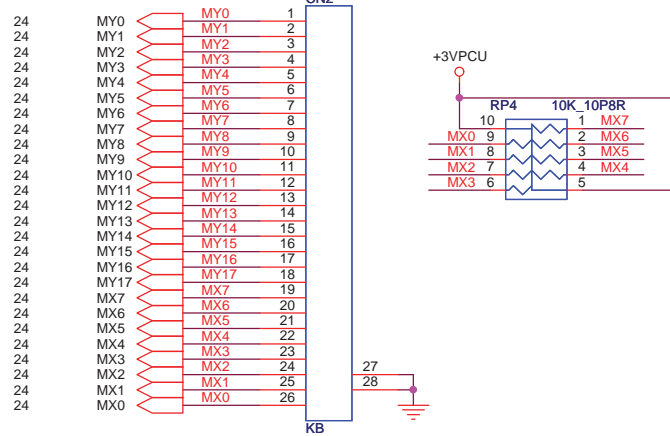
No stuff HOLE9
REV:B 02/17



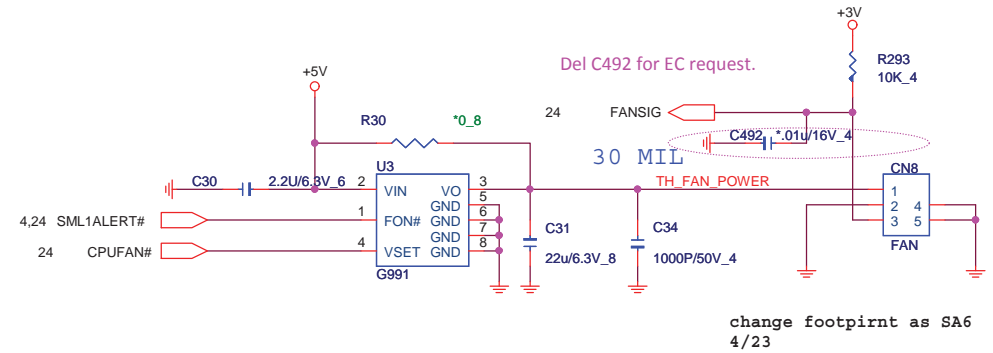
CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 22 of 32

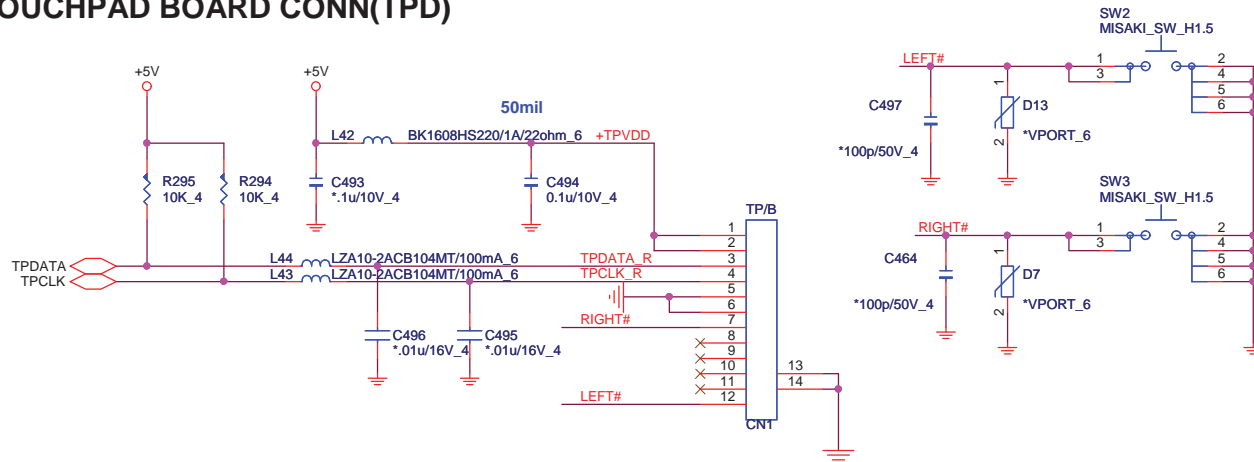
K/B(KBC)



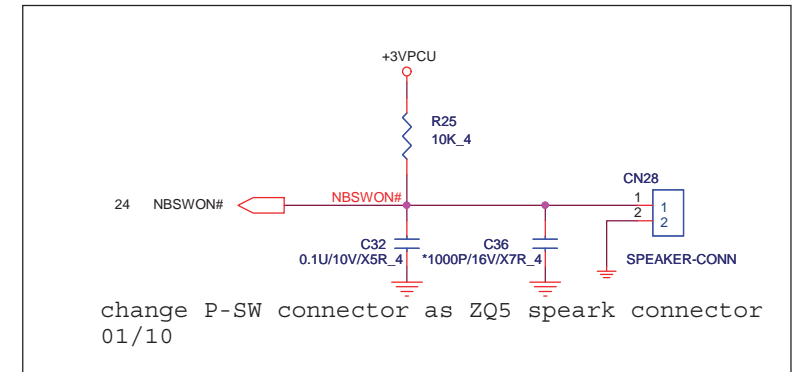
CPU FAN(THM)




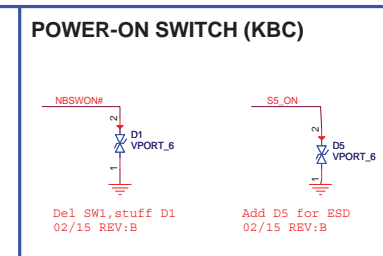
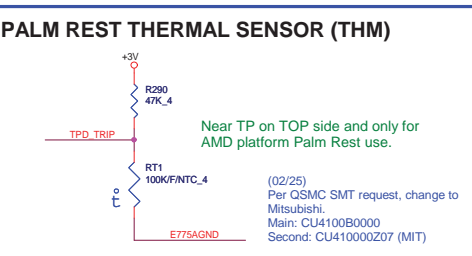
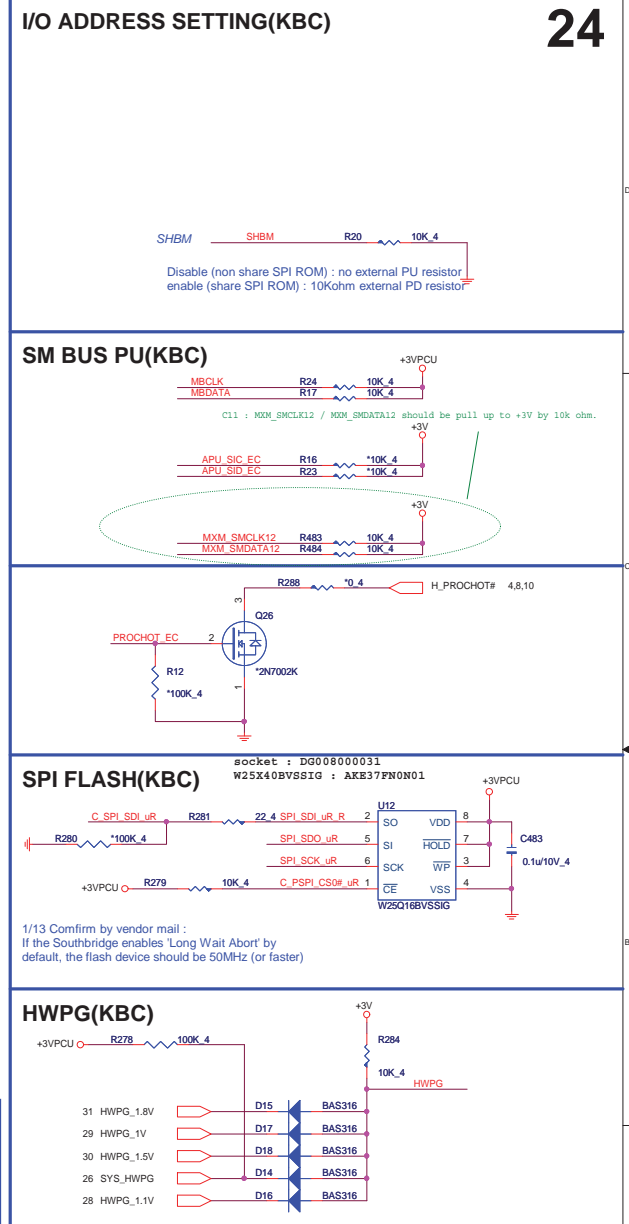
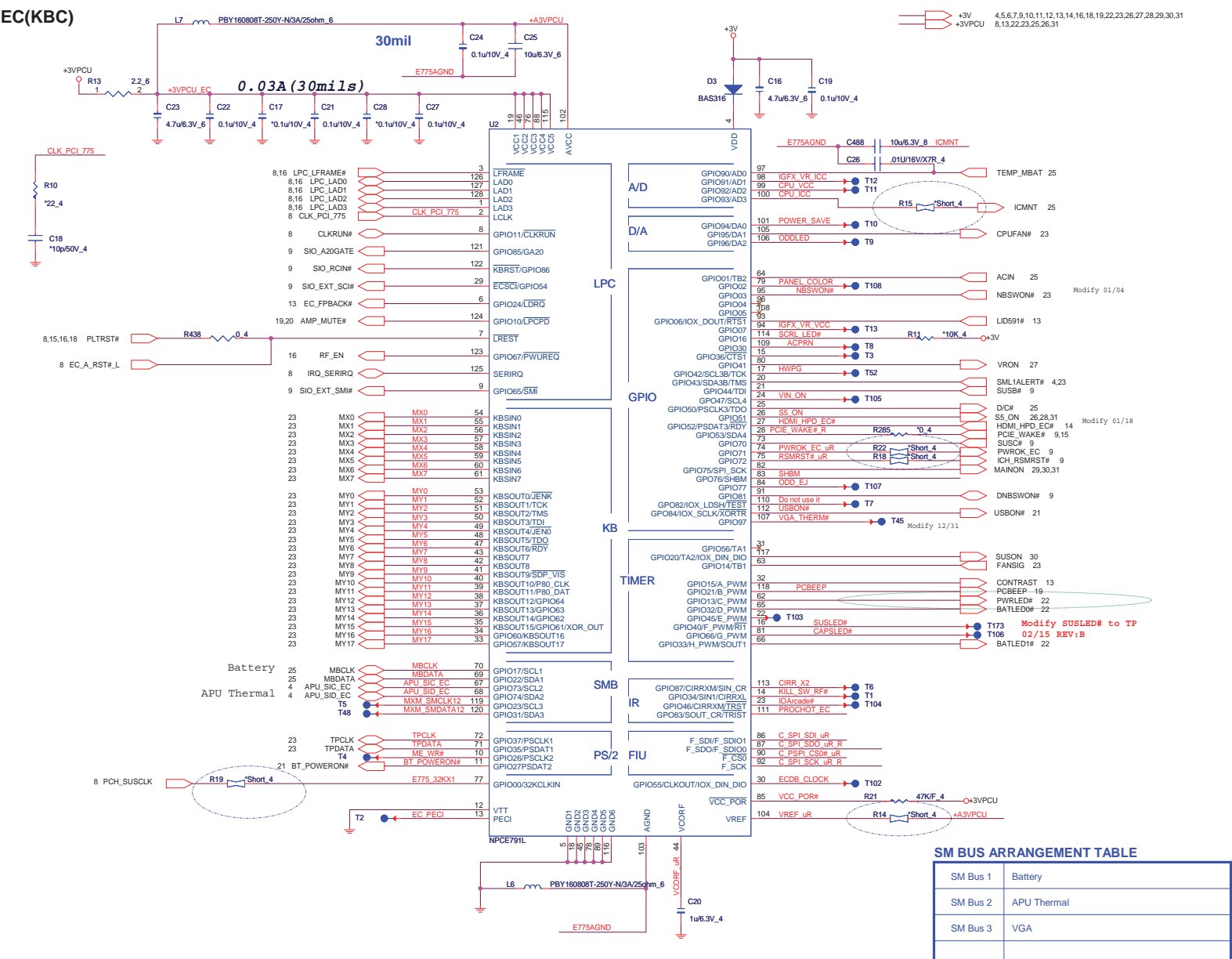
TOUCHPAD BOARD CONN(TPD)



DFFC12FR234 will be EOL by PDC , so change PN to DFFC12FR026



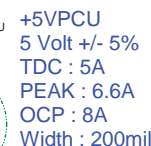
	PROJECT : ZQP Quanta Computer Inc.		
	Size	Document Number	Rev
		KB/TP/FAN	1A
Date:	Tuesday, March 15, 2011	Sheet	23 of 32



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE791 & FLASH	1A
Date:	Tuesday, March 15, 2011	Sheet 24 of 32

SYS_SHDN#  SYS_SHDN# 4,31



+3VPCU
3.3Volt +/- 5%
TDC : 5.02A
PEAK : 6.3A
OCP : 7.5A
Width : 200mil

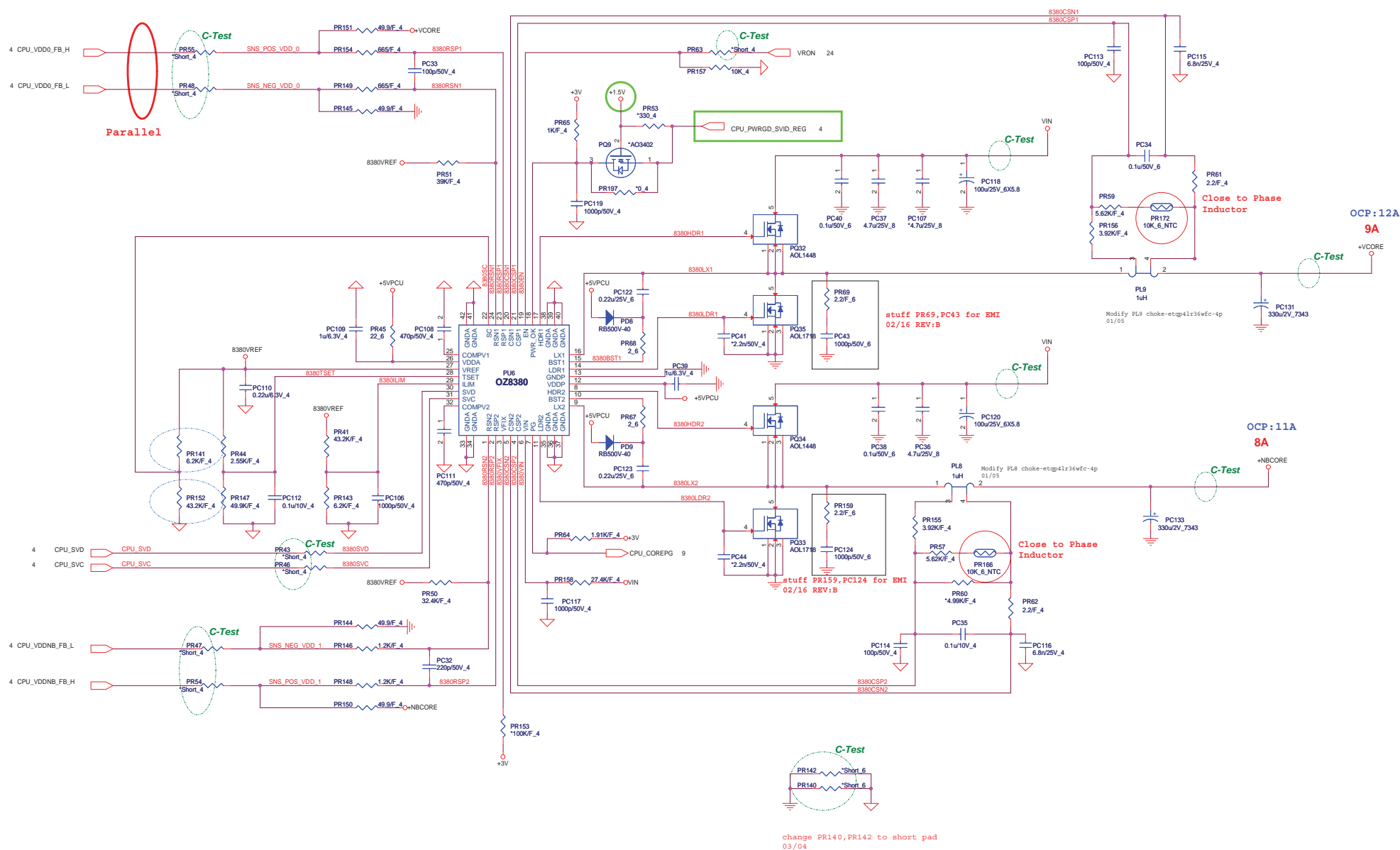
OCP:8A
 $I(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \mu \cdot 0.4 \text{M} \cdot 9) = 2.525 \text{A}$
 $I_{\text{ocp}} = 8 - (2.525/2) = 6.74 \text{A}$
 $V_{\text{th}} = 6.74 \text{A} \cdot 14 \text{m}\Omega = 94.32 \text{mV}$
 $R(\text{Ilim}) = (94.32 \text{mV} \cdot 10) / 10 \mu \text{A} = 94 \text{K}$

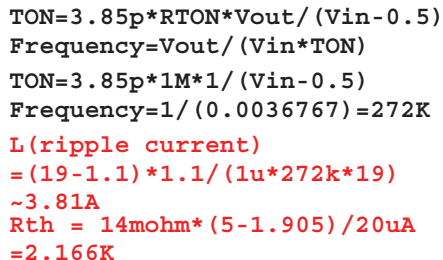
OCP:7.5A
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.5 \text{M} \cdot 9) \sim 1.9 \text{A}$
 $I_{\text{ocp}} = 7.5 - (1.9/2) = 6.55 \text{A}$
 $V_{\text{th}} = 6.55 \text{A} \cdot 14 \text{m}\Omega = 91.7 \text{mV}$
 $R(\text{Ilim}) = (91.7 \text{mV} \cdot 10) / 10 \mu \text{A} \sim 91 \text{K}$

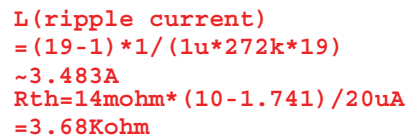


+3V
TDC : 2.48A
PEAK : 3.3A
Width : 100ms

+3V_S5
TDC : 0.62A
PEAK : 0.84A
Width : 40mil

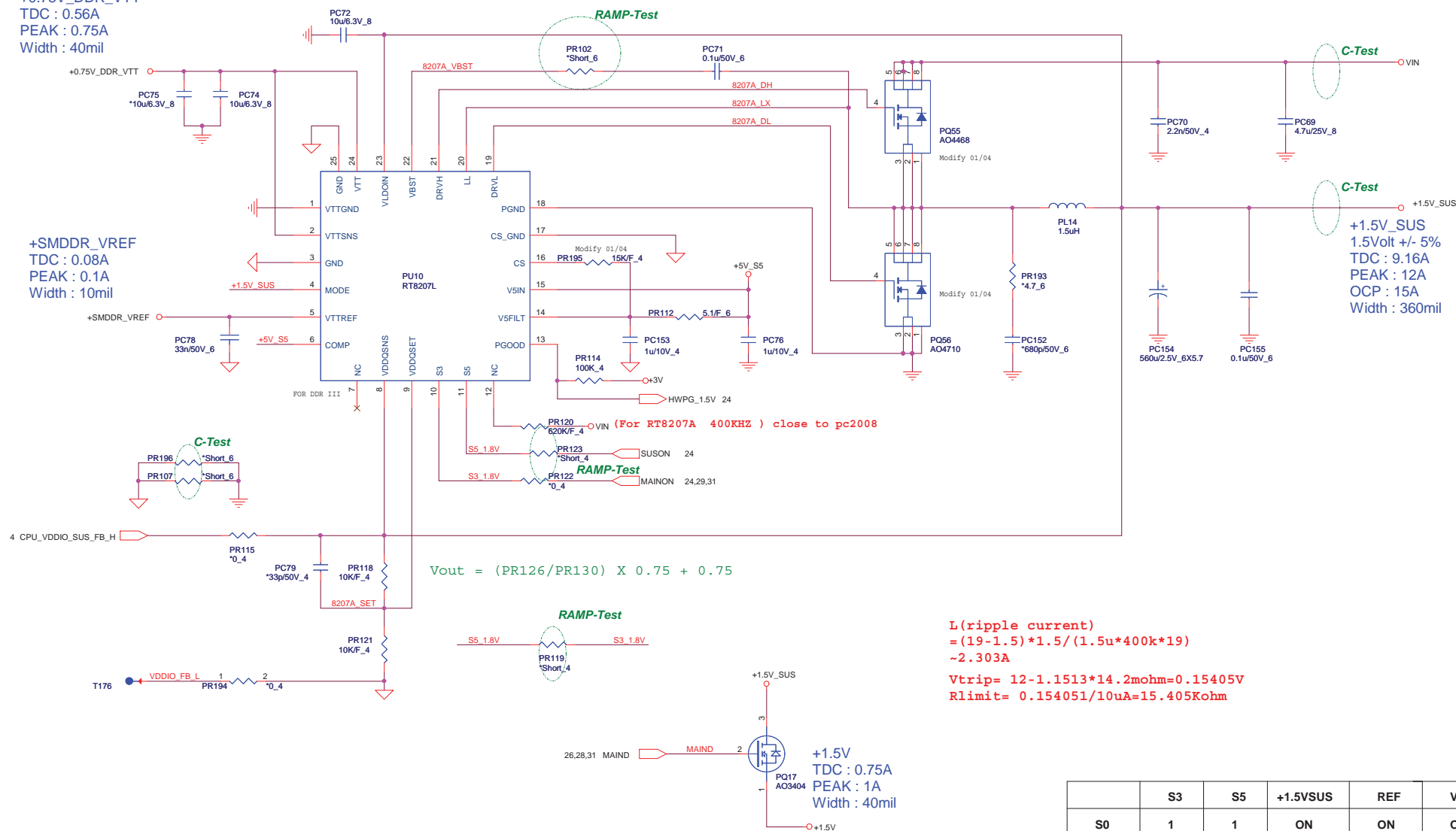






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+0.75V_DDR_VTT
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

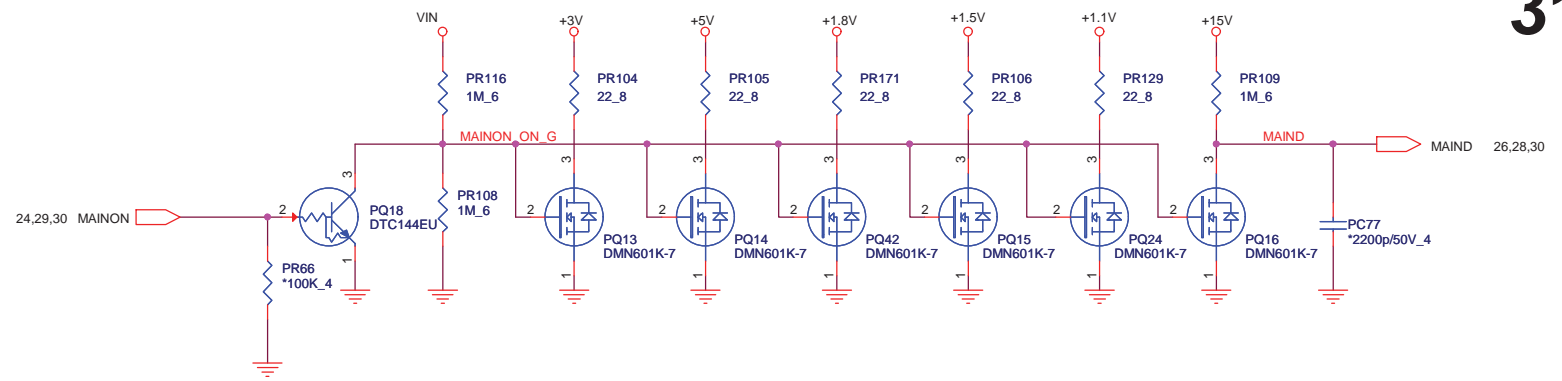


$$V_{out} = (PR126/PR130) \times 0.75 + 0.75$$

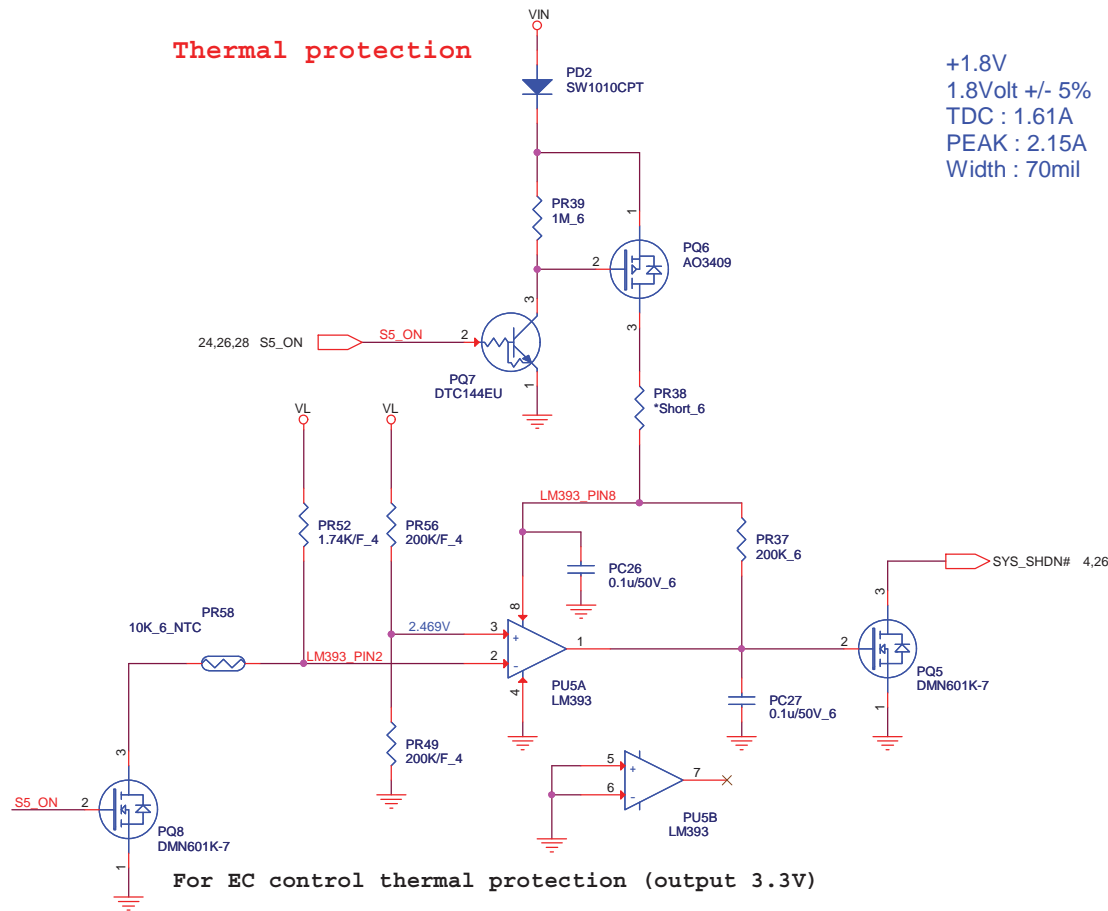
```
L(ripple current)
=(19-1.5)*1.5/(1.5u*400k*19)
~2.303A

Vtrip= 12-1.1513*14.2mohm=0.15405V
Rlimit= 0.154051/10uA=15.405Kohm
```

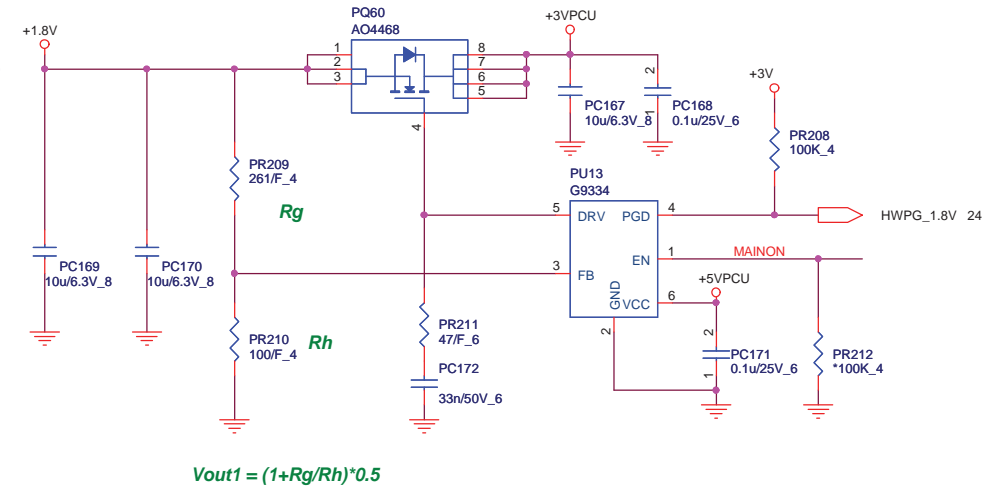
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Thermal protection



+1.8V
1.8Volt +/- 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date:	Tuesday, March 15, 2011	Sheet 31 of 32

MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD			
			Page	From	To	
ZQP/Q M/B	A	First Release	1	1A	3A	
			2	1A	3A	
			3	1A	3A	
<div>01.P14: Add HDMI function</div> <div>02.P22: Add EC53,EC54 for EMI</div> <div>03.P20: Stuff C673/C675/C671/C672 for EMI</div> <div>04.P15: Stuff ESD protector at R31/R32 for EMI</div> <div>05.P10: GPIO 58 define to HDMI strap pin</div> <div>06.P08: Add C606,C614,C619 for strong clock</div> <div>07.P20:change C673,C675,C671,C672 for EMI</div> <div>08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI</div> <div>09.P24:No stuff SW1,stuff D1</div> <div>10.P24:Add D5 on S5_ON for ESD</div> <div>11.P22:LED2 change single lens(blue)</div> <div>12.P08:Del C623</div> <div>13.P24:Del SW1</div> <div>14.P13:Del R26,R27 and add RP5 for EMI</div> <div>15.P15:Add EC38,EC40,EC43,EC46 for EMI</div> <div>16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI</div> <div>17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI</div> <div>18.P27:stuff PR69,PC43 for EMI</div> <div>19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805</div> <div>20.P13:Swap USB nets between L50 and PR5</div> <div>21.P13:Add R33,R34 for ESD</div> <div>22.P15:change C354 to CH122GK1110 for EMI</div> <div>23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI</div> <div>24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237</div> <div>25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140</div> <div>26.P28:Remove JP24,JP25</div> <div>27.P29:Remove JP16,JP17 and change to short pad PR70,PR72</div> <div>28.P30:Remove JP18,JP19 and change to short pad PR196,PR107</div> <div>29.P22:No stuff HOLE9</div>	B	4	1A	3A		
		5	1A	3A		
		6	1A	3A		
		7	1A	3A		
		8	1A	3A		
		9	1A	3A		
		10	1A	3A		
		11	1A	3A		
		12	1A	3A		
		13	1A	3A		
		14	1A	3A		
		15	1A	3A		
		16	1A	3A		
		17	1A	3A		
		18	1A	3A		
		19	1A	3A		
		20	1A	3A		
		21	1A	3A		
		22	1A	3A		
		23	1A	3A		
		24	1A	3A		
		25	1A	3A		
		26	1A	3A		
		27	1A	3A		
		28	1A	3A		
		29	1A	3A		
		<div>01.P15:change RJ45 connector without LED</div> <div>02.P27:change PR140,PR142 to short pad</div> <div>03.P30:change PR119,PR123,PR102 to short pad</div> <div>04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad</div> <div>05.P29:change PR76 to short pad</div> <div>06.P28:change PR79 to short pad</div>	C	30	1A	3A
				31	1A	3A
				32	1A	3A
33	1A			3A		
34	1A			3A		
35	1A			3A		
36	1A			3A		
37	1A			3A		
38	1A			3A		
39	1A			3A		
40	1A			3A		
41	1A			3A		
<div>Quanta Computer Inc. ZQP/Q</div>		PROJECT: ZQP/Q	PCBA NO. http://hobi-elektronika.net	REV: 3A	DOC. NO :	
APPROVED BY : Andy Lin		CHECK BY : JC Huang	DRAWING BY : Andy Chen	DATE :10/18/2010	SHEET 1	